

# A 1.6-3.2GHz, High Phase Accuracy Quadrature Phase Locked Loop

by

Brian P. Ginsburg

Submitted to the Department of Electrical Engineering and Computer  
Science

in partial fulfillment of the requirements for the degree of

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## Abstract

Most PLL research focuses on narrowband systems that support only one communication standard. For a flexible system, it may be desirable to support multiple standards. A single PLL capable of operating over a wide frequency range while meeting all the requirements of the individual standards can save area and design effort, compared with multiple PLLs each supporting only one standard. This thesis presents a PLL that has a very wide tuning range, accurate quadrature outputs, and is geared towards low phase noise. The VCO is identified as the limiting factor in the tuning range and source of the quadrature outputs, as well as the primary source of the phase noise above the loop bandwidth of the PLL, so its design is the principle focus herein.

The VCO uses digitally switched capacitors to extend the tuning range. It consists of two cross-coupled cores that produce quadrature outputs, where phase error arises if the cores are not identical. The VCO's output also has a controlled amplitude and common mode point. The charge pump of the PLL is designed to compensate for variations in the VCO's gain at different frequencies. In simulations using a  $0.13\mu\text{m}$  CMOS process, the VCO achieves a tuning range of 1.585-3.254GHz over process and temperature variations. Its quadrature outputs have less than  $2.6^\circ$  phase error for a 2% mismatch in the capacitance between the two  $LC$ -tanks. The phase noise, calculated assuming a linear, time-variant model, is  $-109.5\text{dBc/Hz}$  at 600kHz offset from 3.217GHz.

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# Chapter 1

## Overview

This thesis focuses on the design and simulation of a wide tuning range, quadrature phase-locked loop. The focus of the design work is on the voltage-controlled oscillator, which limits the tuning range and generates the quadrature outputs.

The first section presents the reasons to develop a PLL that can operate over a wide tuning range and gives the target specifications and constraints for this thesis. It also explains the decision to use an *LC-VCO* instead of a ring oscillator. Section 1.2 describes some of the relevant, existing research; the tuning range extension and quadrature generation techniques in this thesis are derived from works mentioned here. The last section lists the format of the remainder of this thesis.

### 1.1 Motivation

High-speed data communication over both wired and wireless media has become a major area of innovation and research. Increased bandwidth demands have been caused by the rapid growth of the Internet and widespread use of cellular phones. To deliver this bandwidth, new technology has been developed to compress the data, to place the data on the physical medium at higher frequencies, and to receive the appropriate signal accurately. Among the requirements for digital transmission of data is the need to clock both the transmitted and received data. A dedicated clock signal is usually not transmitted with the data, since that would require extra band-

width for a signal that carries no actual information. Thus, clocks must be reliably generated on both ends of the channel. Phase-locked loops (PLLs) are the principal method of clock generation. They have the ability to generate high frequency clock signals from lower frequency ones, perhaps derived from a crystal oscillator, as well as the ability to generate a clock directly from received data. The incredible amount of research about PLLs in the past decade reflects their importance to high-speed communication as well as the large number of challenges that still exist in PLL design and implementation.

Every communication standard places different constraints on the PLL, including different frequency ranges and resolutions, phase noise and jitter requirements, and settling times. In general, most research has gone into producing PLLs that satisfy one specific standard and therefore have limited tuning ranges. With this philosophy, a system that supports multiple standards must therefore include multiple PLLs, which is expensive in terms of die area. For these systems, a single PLL capable of operating over a wide range of frequencies and hence multiple standards, can be extremely useful. Of course, the PLL must still meet all of the other performance requirements of the various standards, or else the wide tuning range is effectively useless.

Another requirement of many communication standards is quadrature clock signals, that is two clocks that differ in phase by  $90^\circ$ . Some encoding schemes (e.g., quadrature phase shift keying) use the two clocks to encode two bits of data at once on the transmission medium. Even if the two phases are not specifically called for by a particular standard, a sine and a cosine wave can be added together to achieve an arbitrary phase signal at the same frequency, so sinusoidal quadrature outputs can be interpolated to achieve more than two phases. This approach is useful if one chip must handle many signals that have the same frequency but potentially different phases. The accuracy of the quadrature outputs is important for both of the above applications. For instance, in QPSK modulation, if a phase error moves the I and Q clock signals away from  $90^\circ$  phase difference, it becomes more difficult to reliably determine both of the transmitted bits, since they will begin to interfere with each

other, increasing the bit-error rate. In the interpolation example, the extra phase signals will not be evenly spaced as phase error increases, so the appropriate phase clock for a certain input may not be available.

In addition to the above two considerations, a high precision clock with low jitter and phase noise is extremely important. For wireless applications, the phase noise of the clock signal directly impacts the spectral purity of any transmitted signal, and narrowband systems in particular must prevent any signal from interfering with adjacent frequency bands. If the clock has significant jitter, the ability to accurately sample digital signals is hampered, leading to increased intersymbol interference and higher bit error rates. This thesis, therefore, is the design of a PLL with a wide tuning range, quadrature outputs, while still maintaining good phase noise performance.

A basic PLL block diagram is shown in Figure 1-1. A phase detector (PD) compares the phase of a reference clock with that of the output clock after its frequency has been divided. This phase difference is then low-pass filtered and used to set the frequency of the VCO. If the reference clock's phase is ahead of the output clock's phase, the VCO will increase in frequency until its phase has caught up. The frequency division in the feedback path allows the output clock frequency to be at an integer multiple of the reference frequency.

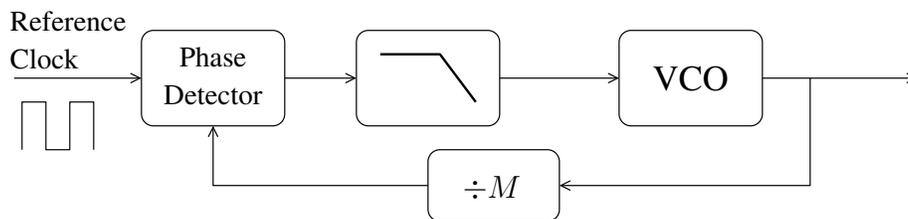


Figure 1-1: Simplified PLL block diagram

The VCO design is the principal focus of this thesis since it has the greatest impact on the three main performance metrics. The VCO is the limiting block to achieve a wide tuning range, since the divider, PD, and filter will operate over the entire range assuming that they function at the highest operating frequency. The VCO is the block that produces quadrature outputs if those are required. Also,

above the loop bandwidth of the PLL, the VCO is essentially running open loop, so it dominates the high frequency phase noise. A great deal of research has already been invested into VCO design and analysis, including tuning range improvements [1-13], quadrature generation [14-26], and phase noise [27-40] of *LC*-oscillators, and the design and phase noise of ring oscillators [41-47].

For modern monolithic VCOs, there are two principal topologies. The first is a ring oscillator, composed of a ring of inverters with a net inversion around the loop, as shown in Figure 1-2. The frequency is inversely proportional to the propagation delay of each of the individual inverters as well as the number of inverters. To tune the frequency of such an oscillator, the propagation delay of an individual stage can be adjusted by varying the current through it [43], or it can be tuned digitally by switching in a different number of inverters. The maximum oscillation frequency of a ring oscillator can be very high since the propagation delay of a self-loaded inverter is small. In fact, ring oscillators are often used to characterize digital processes for precisely this reason. The current through each of the stages can vary over several orders of magnitude, so ring oscillators can have very wide tuning ranges. With differential signalling, a ring oscillator can be built with four stages by flipping the output of the fourth stage as it is fed back to the input of the first stage. In this configuration, the outputs of any two consecutive stages are in quadrature, with any mismatch in the delay through each of the inverters causing phase error; however, if sinusoidal quadrature signals are required, the ring oscillator output must be filtered.

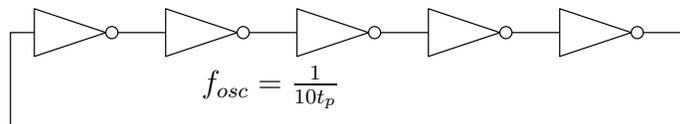


Figure 1-2: 5-stage ring oscillator circuit

The biggest disadvantage of ring oscillators is their poor phase noise performance. As described by Hajimiri in [36], ring oscillators do not store energy from cycle to cycle, so transistors must provide all the energy to charge and discharge the node capacitances every cycle. These active devices are noisy, and insert energy into the

circuit on the clock edges, when the circuit is most sensitive to noise, as opposed to inserting the energy when the output is at a voltage maximum, when any noise will generally not affect the phase noise of the output. The phase noise performance of a ring oscillator will improve by 10dB per decade increase in power consumption [46]. For wireless applications where current draw and resultant battery life are critical specifications, this is generally an unacceptable tradeoff, and even with a significant amount of power, ring oscillators still have poor noise performance.

The other major class of monolithic oscillators is the  $LC$ -oscillator, a subclass of resonant oscillators. The circuit oscillates at the resonant frequency of the inductor and capacitor,  $\omega_0 = 1/\sqrt{LC}$ . In an ideal  $LC$ -tank with no resistive losses, the inductor and capacitor oscillate indefinitely. Since in practice it is impossible to build a lossless passive circuit, active devices are used to produce a negative resistance to cancel out any parasitic losses in the tank, as shown in Figure 1-3.

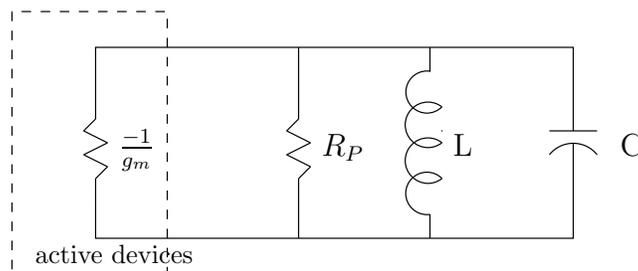


Figure 1-3: Negative resistance model of  $LC$ -oscillators. Stable amplitude oscillations occur when  $-1/g_m = R_P$

The  $LC$ -tank inherently filters out frequencies away from the resonant peak, which improves the phase noise performance, particularly with a high-Q tank. In addition, the energy storage of the inductor and capacitor mean that only a minimum of energy must be added by the active devices, further helping phase noise performance. Most high speed communication systems require an accurate, low jitter clock, and therefore use  $LC$ -oscillators. In the last decade, the usefulness of integrated inductors has made  $LC$ -oscillators inexpensive, especially compared to other resonant oscillators such as those using SAW filters.

The tuning range, though, of  $LC$ -oscillators is generally very limited. Most com-

monly, tuning is accomplished using a varactor as the capacitance in the tank. Since integrated varactors have limited tuning range, and the tuning range of the VCO is only the square root of the tuning range of the varactor,  $LC$ -oscillators cannot compare with ring oscillators in this regard. The standard  $LC$ -oscillator topologies also do not inherently provide quadrature outputs, but some methods to produce quadrature outputs are described in Section 1.2.2. Table 1.1 presents a comparison of the tradeoffs for ring versus  $LC$ -oscillators.

Table 1.1: Ring oscillator versus  $LC$ -oscillator

	Ring oscillators	$LC$ -Oscillators
Tuning range	Very wide, determined by current variation	Narrow, proportional to square root of varactor tuning
Quadrature generation	Inherently produced	Either requires filtering or two coupled VCO cores
Phase noise	Poor	Very good, filtering inherent to $LC$ -tank
Power	Can vary greatly; higher power needed for good phase noise	Cannot be too small, but has lower power for similar phase noise

Extending the limits of  $LC$ -oscillators without sacrificing phase noise performance is the focus of the VCO design. The rest of the PLL is included to demonstrate operation of the VCO over the entire tuning range and to handle the issues of VCO nonlinearity present as the frequency varies. The actual circuit is designed to be part of a more complex real-world system that requires flexibility in its PLL, so the design must work across process and temperature variations. A summary of the design constraints and performance targets is shown in Table 1.2.

## 1.2 Previous Work

This section describes some previous work done on VCOs relevant to this thesis. The first section describes a number of techniques to extend the tuning of a VCO. One of

Table 1.2: Performance Targets and Design Constraints

Process	TSMC 0.13 $\mu$ m CMOS with RF option
Supply Voltage	1.2V
Temperature Range	0°-100°C
Process Corners	All
Tuning Range	1.6-3.2GHz
Phase Error	<3° @ 2% mismatch of $LC$ tank
Phase Noise	-105dBc/Hz at 600kHz offset from 3.2GHz

these techniques forms the basis for the tuning range extension described in Section 2.2. Section 1.2.2 describes the two principal methods of sinusoidal quadrature signal generation using  $LC$ -VCO's.

### 1.2.1 Tuning Range

Noting that the resonant frequency of an  $LC$ -VCO is  $1/\sqrt{LC}$ , there exist a number of techniques to maximize the tuning of both of these passive components. The capacitor is the more traditional tuning element. A new three terminal, gated varactor has been developed with an extended tuning range to replace the standard p-n junction and accumulation mode varactors [8]. This device is implementable in a standard CMOS process and has a tuning range of 0.7 – 2.3pF, greater than  $\pm 50\%$ .

One issue of varactor tuning in modern CMOS processes is the low power supply. If one terminal of the varactor is at a fixed DC bias, then even if the control voltage swings from rail-to-rail, the bias across the varactor only varies by the power supply, 1.2V in this thesis; this often does not allow the varactor to cover its entire tuning range. By adjusting the bias on both terminals of the varactor, the total swing across the capacitor can vary by greater than the supply rail, maximizing its tunability [7]. While both of these approaches can increase the tunability of the oscillator, it is still limited by the fact that no varactor currently can tune by the required 4:1 to allow for a 2:1 tunability of the VCO.

To further enhance the tuning range, the inductor can also be tuned. One method

to tune the inductor is to vary the amount of magnetic coupling between two inductors [10]. Another approach is to have a time varying inductance whose average value can be varied [2]. This latter approach is implemented by splitting the inductor into two parallel inductances, and then placing an NFET in series with one of them, as shown in Figure 1-4. During one period of oscillation,  $M_{N_{ind1}}$  is turned off when the output is above  $V_{ind} - V_{th}$ . By lowering  $V_{ind}$ , the average resistance in series with  $L_2$  increases, which also increases the effective reactance of the tank. The reverse holds if  $V_{ind}$  is raised.

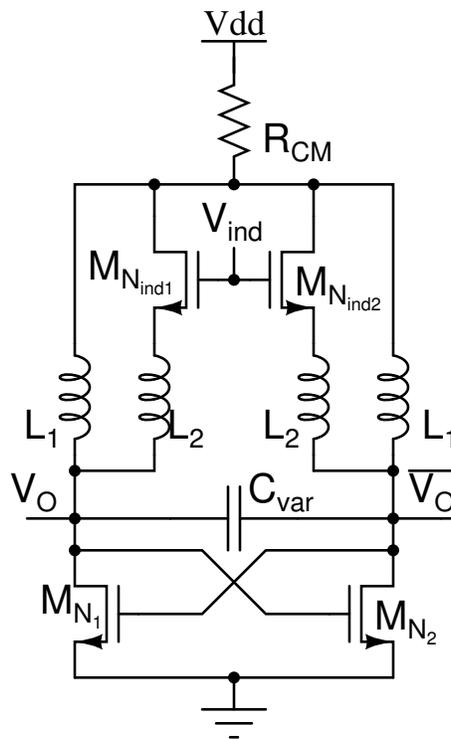


Figure 1-4: Herzel, et al.'s, proposed topology to tune both the inductor and capacitor in an oscillator [2]

This approach, combined with a tunable capacitor has produced a VCO that is tunable from 1.34 to 2.14 GHz, one of the largest published. One disadvantage of this approach is that the output is highly nonlinear because the inductance changes over the period of one oscillation. This makes it unsuitable for applications that need a purely sinusoidal output. In addition, resistance in series with the inductor increases



## 1.2.2 Quadrature Generation

Given an  $LC$ -VCO with sinusoidal outputs, one way to generate quadrature outputs is to filter the signal. The simple RC-CR network of Figure 1-6 has  $I$  and  $Q$  outputs ideally with  $90^\circ$  of phase difference between them, but phase error occurs if the values of the resistors and capacitors are not matched. In addition, the  $I$  and  $Q$  outputs have different amplitudes if the input frequency is not precisely at  $1/(2\pi RC)$ . To overcome this limitation, more complex polyphase filters have been developed that produce equal amplitude outputs over a wider range of frequencies [48]. These filters are passive and lossy, which hurts phase noise performance. In addition, buffers are needed on both their inputs and outputs, which may significantly increase the total power budget.

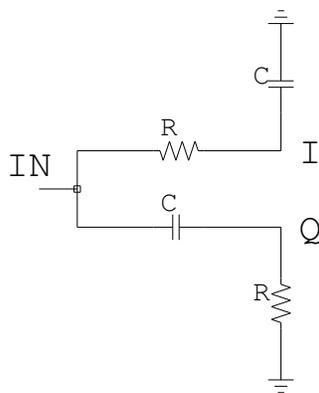


Figure 1-6: RC-CR network that produces quadrature outputs

More recently, Rofougaran has developed a topology that can directly produce quadrature outputs from an  $LC$ -VCO. This topology couples two identical VCO cores together to produce two differential outputs that are  $90^\circ$  apart [21]. Schematics and block diagrams of this topology, as well as a theoretical analysis of its operation can be seen in Section 2.3. The phase accuracy of the outputs is dependent upon the matching between the resonant tanks, and given some mismatch between the tanks, higher coupling between the tanks decreases the phase error. Many circuits have been presented that use this topology or variants thereof for quadrature generation [7, 20, 22, 23].

## 1.3 PLL Design Overview

The next chapter describes the design of the VCO. The tuning range is extended using digitally switched capacitors, and the tradeoffs involved in the design of these switches is discussed in more detail. The VCO contains three main control loops: a quadrature generation control loop, a control loop to set the common mode point of the output, and a biasing loop to produce constant amplitude oscillations under a variety of operating conditions. This last loop is also responsible for ensuring startup of the VCO. The design and stability analysis of all three loops is described. A theoretical explanation of the operation of the quadrature control loop and a prediction of the phase error given mismatch between the cores is also included.

Chapter 3 presents the design of the PLL as a whole, including all of the components besides the VCO. The PLL is not designed to have a particularly high frequency resolution on its output, as a divider is used that can only divide by eight or sixteen. Thus the reference frequency on the input can vary from 100MHz to 400MHz. The PLL is Type II, which means that its loop filter has an integrator for zero steady-state error, as well as a zero to ensure stability.

A slightly modified tristate phase-frequency detector is used, implemented entirely in current-mode logic to reduce noise coupling onto the supply and into the substrate from the digital circuitry. All of the signalling throughout the PLL, except for the control voltage input to the VCO is differential.

The VCO has a non-linear tuning characteristic, with the gain of the VCO increasing at lower frequencies when more capacitors are switched in. The charge pump compensates for this variation to produce constant PLL loop dynamics over all frequencies of operation.

The results of the simulations of the VCO and PLL can be seen in Chapter 4. All of the specifications listed in Table 1.2 are met, but the phase noise performance degrades at lower frequencies, the opposite of what generally happens in VCOs, because of added loss in the resonant tank.

Finally, Chapter 5 reviews the principal contributions of this thesis and summa-

rizes the design of the PLL and the simulation results. It also includes a number of suggestions for future work using the ideas presented herein.

# Chapter 2

## Voltage-Controlled Oscillator

### Design and Analysis

The VCO, with overall block diagram as shown in Figure 2-1, is composed of two cross-coupled differential  $LC$  cores. These cores each have a set of 22 capacitor banks to allow coarse digital tuning for a wider available frequency range. The output amplitude of the VCO is sensed using a peak detector, and  $V_{IBIASCTL}$  is set by the amplitude control loop so that the measured amplitude  $V_{PEAK}$  matches a reference voltage  $V_{REFPEAK}$ . To maximize the tuning range of the varactors as  $V_{CTL}$  varies, the average output common mode voltage of the two cores,  $V_{TAPCM}$ , is fixed at 0.65V by a common mode control loop. This loop operates by setting  $V_{CMCTL}$ , which changes the impedance of the pullup devices; a higher  $V_{CMCTL}$  increases their impedance and lowers the output common mode voltage.

The first section describes the simple VCO core, which forms the basis of all subsequent sections. Section 2.2 presents the design of the capacitor banks to produce sufficient tuning range. Section 2.3 describes the modification to the simple VCO core to generate quadrature output clocks, including a theoretical analysis of the quadrature control loop and phase response to tank mismatch. The quadrature loop ideally can function in two modes, with the phase shift between the cores as  $\pm 90^\circ$ . One of these two modes, however, is unstable, and two circuit designs are described to force the VCO into the stable quadrature mode of operation.

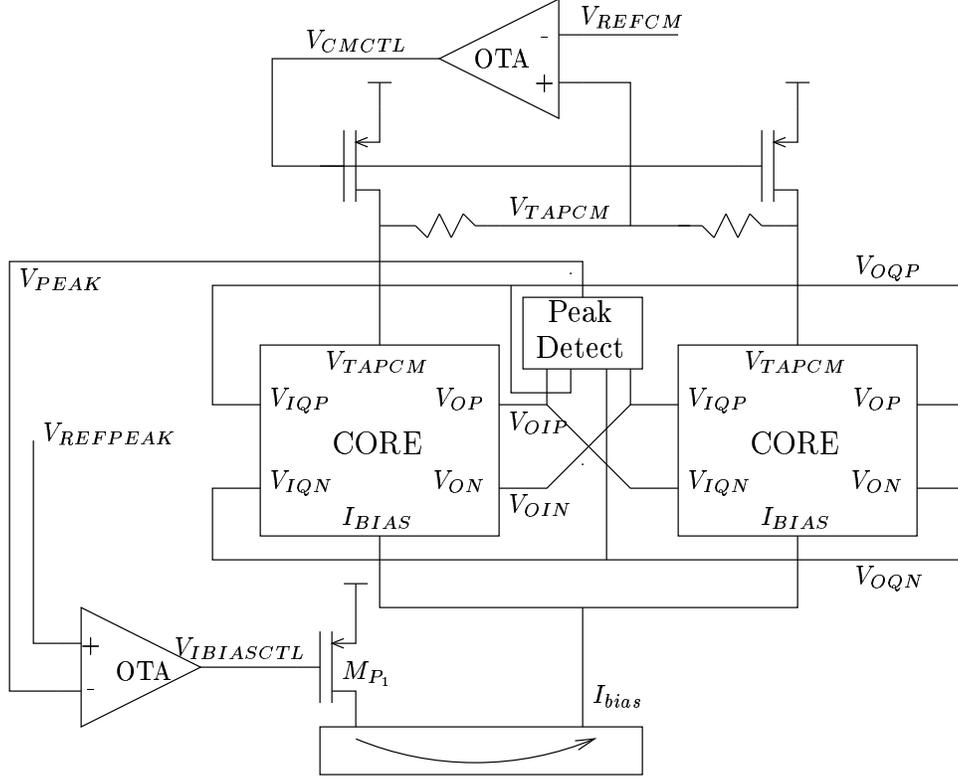


Figure 2-1: Overall VCO block diagram

The common mode and amplitude control loops are discussed in Sections 2.4 and 2.5, respectively. These two loops do not function completely independently, and a stability analysis of their interaction is also included. Section 2.6 presents the operational transconductance amplifier that is used in both of those control loops, and the chapter concludes with a summary of the major design choices.

## 2.1 Core

The VCO in this design is based on the simple differential topology with an  $LC$  tank, as seen in Figure 2-2. The tank can be modelled as an inductor, a lumped capacitor (including parasitic capacitance from the active devices), and a parasitic resistance  $R_P$  from the non-ideal inductor and capacitors.

The cross-coupled NMOS transistors  $M_{N1}$  and  $M_{N2}$  are used to cancel out the loss in the tank. Noting that  $v_{o1} = -v_{o2}$  and  $ICOM$  is a small signal differential ground,

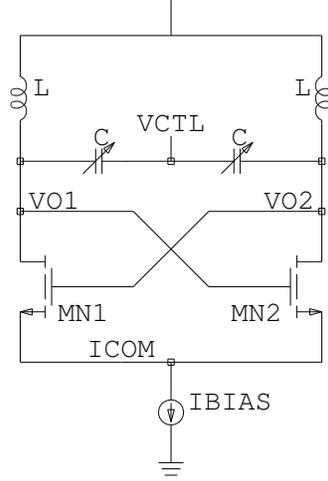


Figure 2-2: Simple differential  $LC$  VCO core

then  $v_{gs1} = v_{o2} = -v_{o1}$ , and the incremental current through  $M_{N1}$  is  $i_{d1} = -g_m v_{o1}$ . Therefore, the impedance looking down into the drain of  $M_{N1}$  is  $v_{o1}/i_{d1} = -1/g_m$ . Thus, in order to ensure constant amplitude oscillations, this negative resistance must equal the parasitic resistance:

$$-1/g_m = R_P \quad (2.1)$$

If  $g_m$  is too low, any oscillations will decrease in amplitude, while if  $g_m$  is too high, any oscillations will grow exponentially. To achieve constant amplitude oscillations with this topology, the non-linearity of the transistors is exploited. As the amplitude of oscillation increases, the effective  $g_m$  of the active devices decreases due to the active devices entering triode for part of the oscillation period. In order to ensure startup of the oscillator, the  $g_m$  is chosen to produce a startup gain between 2 and 3. Then, any initial perturbation grows exponentially, decreasing  $g_m$ , until a stable amplitude is reached.

## 2.2 Tuning Range Design

Tuning of the simple VCO core of Figure 2-2 is accomplished by setting  $V_{CTL}$ , which changes the voltage across the varactors. The oscillation frequency is  $f_0 =$

$1/(2\pi\sqrt{LC})$ , where  $C$  is the tunable capacitance of the varactor plus the fixed capacitances from the transistors, interconnect, and inductor. As mentioned in Section 1.1, this topology cannot yield a wide enough tuning range using today's varactors.

To achieve a wider tuning range, the method proposed by Kral in [4] is used. By digitally switching in capacitors, the tuning range can be extended far beyond that possible from a single capacitor. This produces a circuit that is capable of coarse tuning by choosing the appropriate capacitors to switch in, but is still capable of fine tuning using varactors. This VCO has a set of twenty-two capacitor banks, activated in a thermometer fashion: to go lower in frequency, sequentially more capacitor banks are activated. More specifically, the switched capacitors are  $C_0, C_1, \dots, C_{21}$ , such that if  $C_i$  is switched in, then all capacitors,  $C_0, \dots, C_{i-1}$  are also switched in.

The actual switched capacitor bank is shown in Figure 2-3, where  $M_{P1}$  and  $M_{N1}$  form a transmission gate connecting the capacitor to one core node, while  $M_{P2}$  and  $M_{N2}$  connect to the other node. The signals  $D_P$  and  $D_N$  are complementary, rail-to-rail control signals. The  $V_{CTL}$  voltage can vary almost rail-to-rail, so that both the NMOS and PMOS devices are needed to prevent the transmission gate from turning off. The capacitors  $C_5$  and  $C_6$  are n-well varactors with  $C_{max}/C_{min} \approx 3.5$ , and a maximum  $\frac{\partial C}{\partial V}$  of 375fF/V for a 350fF varactor. The actual tuning curve of the varactor is shown in Figure 2-15, as part of the discussion of the common mode control loop.

When turned on, the transmission gate transistors operate in the triode region, so the effective conductance across the gate is

$$g_{trgate} = C_{OX} \left( \mu_n \frac{W_n}{L_n} (V_{DD} - V_{CTL} - V_{tn}) + \mu_p \frac{W_p}{L_p} (V_{CTL} + V_{tp}) \right), \quad (2.2)$$

where  $C_{OX}$  is the capacitance per unit area of the gate oxide,  $\mu_n$  and  $\mu_p$  are the mobility of electrons and holes, respectively,  $W$  and  $L$  are the width and length of the transistor, and  $V_t$  is the threshold voltage. In order for the Q of the VCO tank to be as high as possible, this conductance, and hence  $W_n$  and  $W_p$ , must be large; however, the parasitic capacitance of the transistor is proportional to its width,

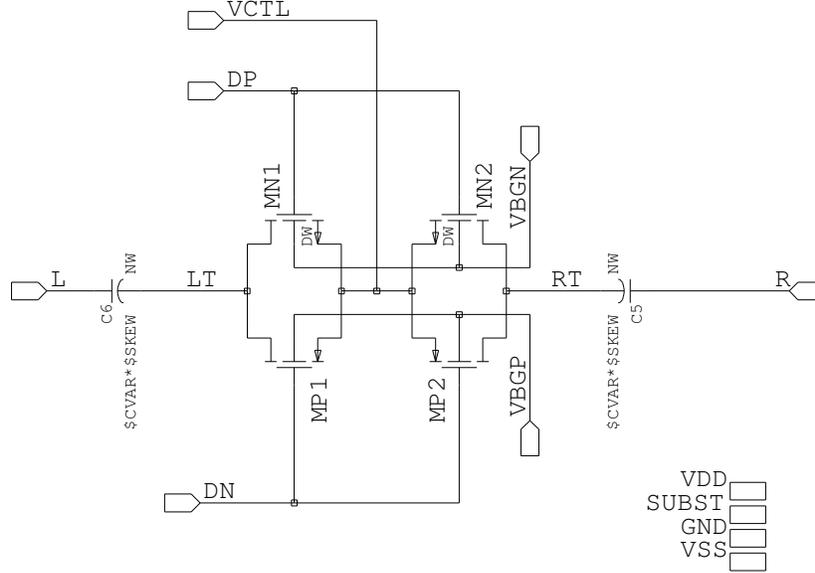


Figure 2-3: One bank in the capacitor array

leading to large parasitic capacitance on the VCO tank node and lowering the overall maximum frequency of the oscillator.

To increase the conductance without adding capacitance, the backgate voltage is adjusted using  $V_{BGN}$  and  $V_{BGP}$ . The NMOS transistors are deep N-well devices, so their backgate can be adjusted. By raising the backgate, the threshold voltage is reduced according to

$$V_{tn} = V_{tn0} + \gamma(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}), \quad (2.3)$$

The backgate of the PMOS transistor is lowered from  $V_{DD}$ , which correspondingly decreases the magnitude of  $V_{tp}$ .

The drawback to adjusting the backgate is that the pn junctions between the backgate and the drain and source diffusions can become forward biased. In the final design,  $V_{BGN} = 0.4V$  and  $V_{BGP} = 0.8V$ . The maximum  $V_{CTL}$  swing from the control buffer described in Section 3.5 is 0.1 to 1.1V, forward biasing the source diffusion to backgate diodes by about 0.3V. These forward biased diodes draw less than 1nA per transmission gate over the achievable  $V_{CTL}$  range, as shown in Figure 2-4. The final

conductance of the transmission gates versus the control voltage is shown in Figure 2-5. At low values of  $V_{CTL}$ , the NMOS transistor dominates, while at higher values of  $V_{CTL}$ , the PMOS transistor dominates, with the transition between the two at 0.73V, the minimum conductance point. The overall Q of the tank, therefore, is higher at the extremes of  $V_{CTL}$ , and lowest in the midpoint of the control voltage.

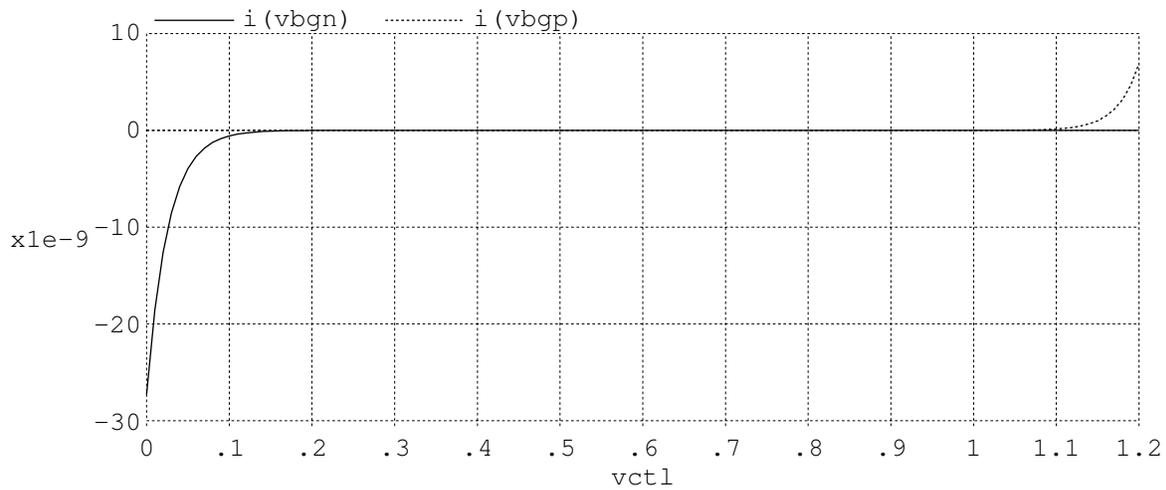


Figure 2-4: Backgate current, in amperes, through one switch as  $V_{CTL}$  varies

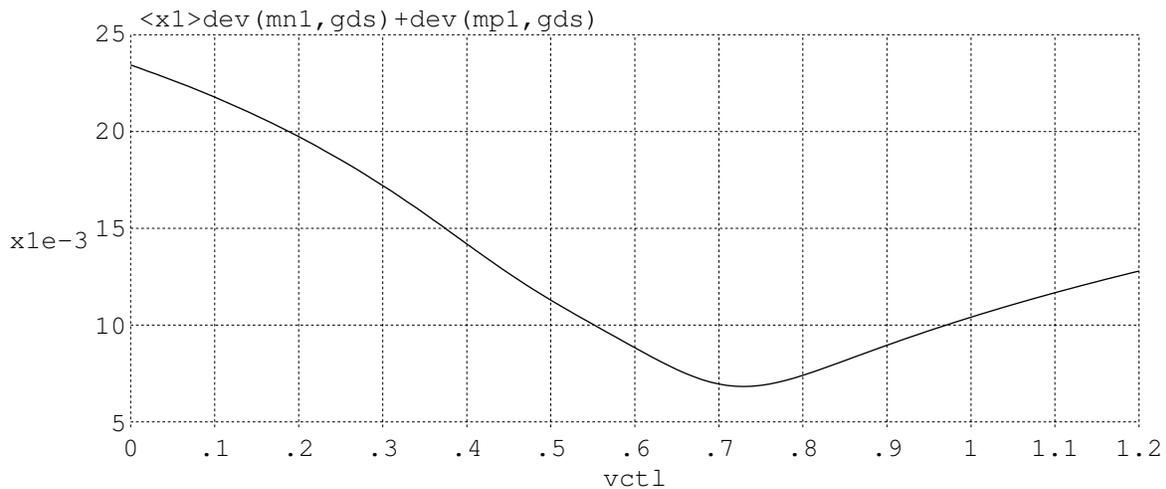


Figure 2-5: Total admittance, in siemens, through one switch as  $V_{CTL}$  varies

The final part of the tuning range design is frequency overlap between successive banks. The fine tuning range must be greater than the jump in frequency from switching in another capacitor. To guarantee a high enough tuning range, varactors

provide the capacitance in each bank, so that the tuning range increases as the coarse tuning switches in more banks. This approach has two disadvantages. The varactors available in the process have more parasitic capacitance than the high selectivity MiMcaps; however, the parasitic capacitance is not symmetric. By placing the majority of these parasitics on the lower frequency control voltage node, the maximum oscillation frequency is not affected significantly. The other problem is that  $K_{VCO}$ , the gain of the VCO measured in Hz/V, increases as more varactors are activated. Since  $K_{VCO}$  affects the PLL loop dynamics, explicit compensation is used as described in Section 3.3.1.

## 2.3 Quadrature Generation

While the VCO presented at the start of this chapter inherently produces signals  $180^\circ$  out of phase, it cannot produce quadrature outputs directly. A topology that uses two of these cores, however, can produce quadrature outputs. This topology, shown in Figure 2-6, stems from work by A. Rofougaran [21] and is the primary method for generating quadrature outputs directly from an *LC*-VCO.

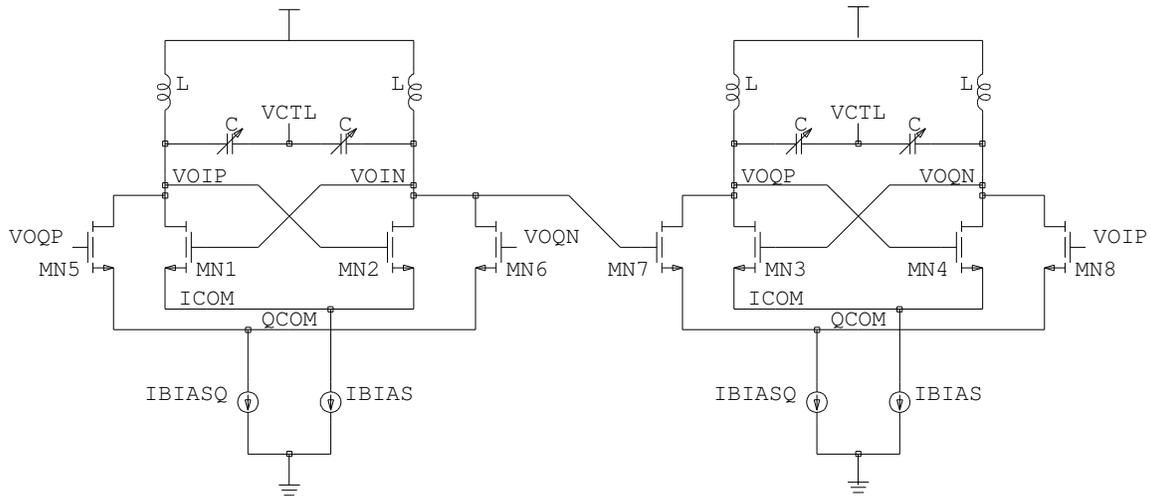


Figure 2-6: Basic quadrature schematic

The transistors  $M_{N1} - M_{N2}$ ,  $M_{N5} - M_{N6}$  and  $M_{N3} - M_{N4}$ ,  $M_{N7} - M_{N8}$  form two identical cores.  $M_{N1}$  and  $M_{N2}$  act as restorative devices, cancelling out losses in the

tank (the same as in the topology of Figure 2-2). The two additional transistors in each core act to couple in the signals from the other core. The left core is cross coupled into the right core, and the right core is directly coupled to the left core.

### 2.3.1 Theory of Operation

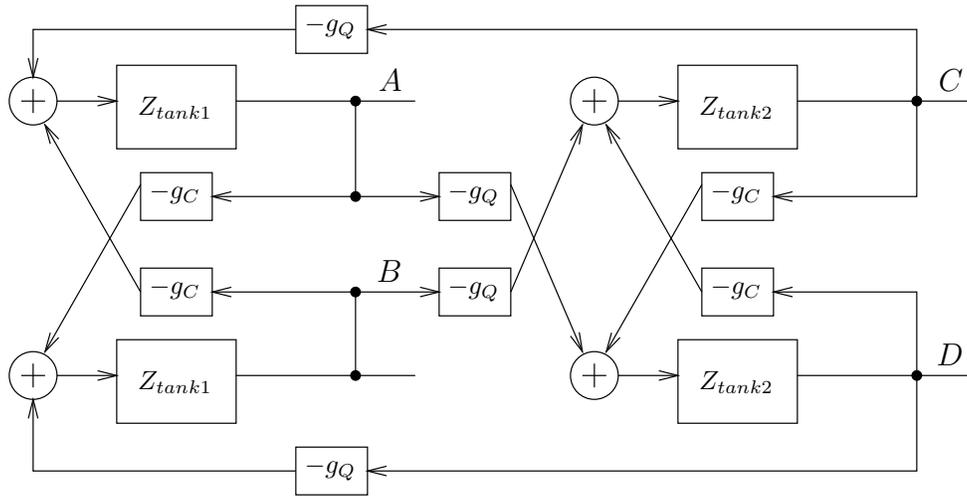


Figure 2-7: Linear quadrature model. A and B are the outputs of one core, and C and D are outputs of the other.

Assuming that the transistors in the the two cores are identical, the transconductance of the regenerative devices is  $g_C$ , and the transconductance of the coupling devices is  $g_Q$ , the quadrature control loop then can be modelled as shown in Figure 2-7. The following equations, paralleling a similar proof in [25], define the behavior of this oscillation:

$$\begin{aligned}
 A &= (-g_C B - g_Q C) Z_{tank1} \\
 B &= (-g_C A - g_Q D) Z_{tank1} \\
 C &= (-g_C D - g_Q B) Z_{tank2} \\
 D &= (-g_C C - g_Q A) Z_{tank2}.
 \end{aligned}
 \tag{2.4}$$

If the tanks are identical ( $Z_{tank1} = Z_{tank2} = Z_{tank}$ ), these equations are equivalent to

the following matrix equation:

$$\begin{bmatrix} 1 & g_C Z_{tank} & g_Q Z_{tank} & 0 \\ g_C Z_{tank} & 1 & 0 & g_Q Z_{tank} \\ 0 & g_Q Z_{tank} & 1 & g_C Z_{tank} \\ g_Q Z_{tank} & 0 & g_C Z_{tank} & 1 \end{bmatrix} \begin{bmatrix} A \\ B \\ C \\ D \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (2.5)$$

Since the desired VCO output is non-zero, the determinant of the square matrix must be zero, which yields

$$1 - 2g_C^2 Z_{tank}^2 + 4g_C g_Q^2 Z_{tank}^3 + g_C^4 Z_{tank}^4 - g_Q^4 Z_{tank}^4 = 0. \quad (2.6)$$

To solve this equation, let  $G = g_C Z_{tank}$  and  $m = g_Q/g_C$ . Then, Equation 2.6 becomes

$$1 - 2G^2 + 4m^2 G^3 + (1 - m^4)G^4 = 0. \quad (2.7)$$

Assuming that  $m \neq 1$ , then the four solutions are

$$G = \frac{-1}{1 \pm m}, \frac{1}{1 \pm jm}. \quad (2.8)$$

A quadrature solution also exists if  $m = 1$ , but since it is practically impossible for  $g_Q$  to precisely equal  $g_C$ , this case is ignored. Rewriting Equation 2.4 in terms of  $A$ ,  $G$ , and  $m$ , yields

$$\begin{aligned} A &= A \\ B &= \frac{-G+m^2 G^2+G^3}{1-G^2+m^2 G^3} A \\ C &= \frac{2mG^2-m^3 G^3}{1-G^2+m^2 G^3} A \\ D &= \frac{-mG-mG^3}{1-G^2+m^2 G^3} A. \end{aligned} \quad (2.9)$$

Substituting in the complex solutions,  $G = 1/(1 \pm jm)$  from Equation 2.8 yields the

following relationship:

$$\begin{aligned}
A &= A \\
B &= -A \\
C &= \mp jA \\
D &= \pm jA,
\end{aligned} \tag{2.10}$$

which means that the four outputs are in quadrature.

With this quadrature topology, the output is no longer fixed at  $\omega_0 = 1/\sqrt{LC}$ . To satisfy the constraint that  $G = 1/(1 \pm jm)$ , one gets

$$g_C Z_{tank} \cdot (1 \pm jm) = 1. \tag{2.11}$$

There are two potential oscillation frequencies, where  $\phi(g_C Z_{tank}(j\omega_1)) = \tan^{-1}m$  and  $\phi(g_C Z_{tank}(j\omega_2)) = -\tan^{-1}m$ . The transconductance  $g_C$  is assumed to be real, so then the oscillation frequency solely depends on the phase of the tank impedance.

Assuming the loss in the tank is primarily from a parasitic resistor in series with the inductor, the tank impedance is

$$\begin{aligned}
Z_{tank} &= \frac{R+L\omega j}{1+RC\omega j-LC\omega^2} \\
&= \frac{R+L\omega j}{(j\omega - (\frac{R}{2L} + j\frac{1}{\sqrt{LC}}\sqrt{1-\frac{R^2C}{L}}))(j\omega - (-\frac{R}{2L} - j\frac{1}{\sqrt{LC}}\sqrt{1-\frac{R^2C}{L}}))}
\end{aligned} \tag{2.12}$$

A plot of this tank impedance is shown in Figure 2-8, with the locations of  $\omega_1$  and  $\omega_2$  for  $m = 0.53$  labelled.

According to the above derivation, there are two modes of operation for the VCO,  $M_1$  and  $M_2$ , corresponding to the frequencies  $\omega_1$  and  $\omega_2$ , both of which are stable solutions. In mode  $M_1$ , the output of the second tank,  $C - D$ , is  $90^\circ$  ahead of the output of the first tank, and in mode  $M_2$ , the first tank leads the second tank by  $90^\circ$ . This means that given a certain control voltage and bank selection, the VCO can operate with a phase difference of  $\pm 90^\circ$  and two potentially very different frequencies. For the tank impedance of Figure 2-8, this frequency difference is over 900MHz. A lower  $m$  or a higher  $Q$  of the tank will decrease this difference, but a lower  $m$  makes

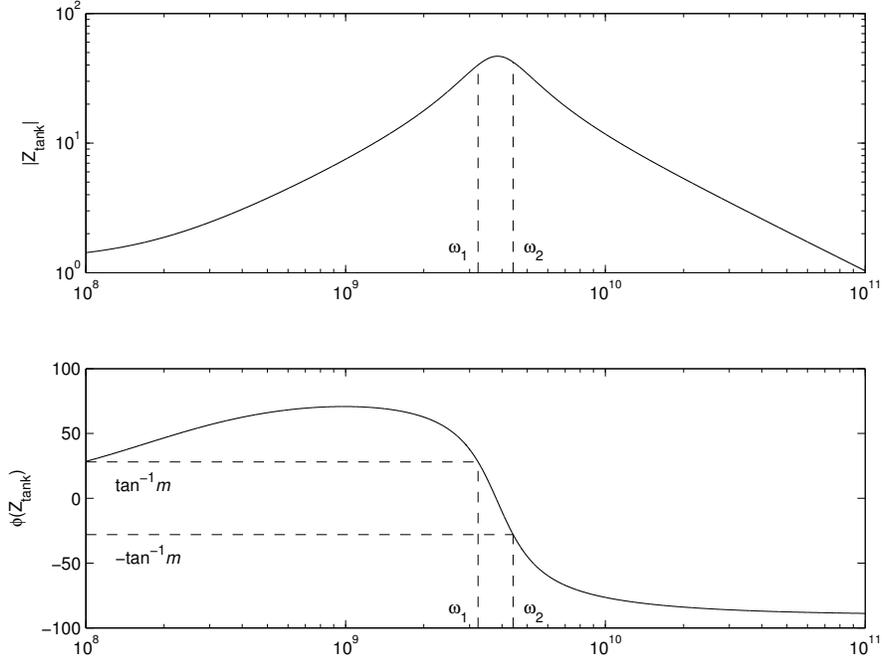


Figure 2-8: Magnitude and phase of the tank impedance, including the location of the quadrature oscillation frequencies with  $m = 0.53$ .

the VCO phase accuracy more sensitive to mismatch between the cores, and  $Q$  is limited by process parasitics beyond the control of the circuit designer. Therefore, for the VCO to ensure coverage of the entire frequency range of 1.6–3.2GHz, it must be capable of operating over a much larger frequency range, so that given operation in arbitrary mode  $M_1$  or  $M_2$ , the VCO still covers the target range.

Simulations, though, showed that  $M_2$ , the higher frequency mode, is not always stable. If there is a lot of loss in the tank, such as in the lower frequency banks, or if  $m$  is high, the VCO may start up in mode  $M_2$  but will switch to  $M_1$ . If the VCO starts up in  $M_1$ , it never switches to  $M_2$ . Unfortunately, even this behavior cannot be relied upon because the tank is less lossy at the higher frequency banks, so an  $m$  sufficient to force the VCO into  $M_1$  at lower frequencies may be insufficient at higher frequencies. It is possible to set  $m$  sufficiently high to always force the VCO into  $M_1$ , but that requires a lot of current through the quadrature coupling transistors. Sections 2.3.4 and 2.3.5 describe two approaches to force the VCO into quadrature mode  $M_1$  without making  $m$  unnecessarily high in steady-state.

The reason that  $M_2$  is not a stable mode of oscillation has to do with neglected parasitics. When  $m$  is high and the  $Q$  of the tank is low,  $\omega_2$  is much higher in frequency than  $\omega_1$ , and also much higher in frequency than  $\omega_0 = 1/\sqrt{LC}$ , the resonant frequency of the tank. With  $m = 1$ ,  $\omega_2 = \omega_0 + 7.6 \times 10^9 \text{ rad/s}$ . At these high frequencies, the loop gain is lessened significantly by parasitic poles. Once the loop gain falls enough, the amplitude control loop is not able to set  $g_C$  high enough to compensate, and the VCO output begins to die; however, since the gain at  $\omega_1$  is not affected by these higher frequency parasitics, the VCO then switches into mode  $M_1$ , where there is sufficient gain to maintain oscillations.

### 2.3.2 How Quadrature Loop Affects Phase Noise

The quadrature loop changes the phase noise performance from a simple VCO in three principal ways. The coupling devices are additional noise sources that can be significant contributors for large  $m$ . Since the VCO does not oscillate at the point where the tank impedance is at a maximum, the transconductance through the regenerative devices is increased, affecting their noise contributions. Another effect of oscillating away from the resonant peak of the tank is that the inherent filtering of the tank upon the phase noise is changed.

In the following analysis, a linear, time-invariant model of phase noise is assumed for simplicity. The actual phase noise measurements of Section 4.2.6 use a linear time-variant model. The phase noise of a resonant oscillator operating at the peak of its tank impedance, in the  $1/f^2$  region of operation can be shown to be

$$\mathcal{L}(\Delta\omega) = 10 \log \left( \frac{1}{2} \cdot \frac{\overline{i_n^2}}{i_{sig}^2} \left( \frac{1}{2Q} \frac{\omega_0}{\Delta\omega} \right)^2 \right), \quad (2.13)$$

where  $\overline{i_n^2}$  is the total noise current power,  $i_{sig}^2$  is the squared rms carrier current, and  $Q$  is the quality factor of the tank.

The total noise current power consists of a contribution from the thermal noise of

the parasitic resistance in the tank and the total noise from all of the active devices:

$$\overline{i_n^2} = \overline{i_{nR}^2} + \overline{i_{nd}^2}. \quad (2.14)$$

The noise from the active devices above the  $1/f$  noise corner is the drain current noise

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f, \quad (2.15)$$

where  $\gamma$  is the process dependent excess noise factor and  $g_{d0}$  is the transconductance at zero  $V_{DS}$  and is proportional to  $g_m$  (i.e.,  $g_{d0} = g_m/\alpha$ ) [49]. This simplified noise model ignores the gate noise of the transistor. Let the transconductance of a simple, non-quadrature VCO core be  $g_{C0} = 1/Z_{tank}(j\omega_0)$ . Since the thermal noise of the parasitic tank resistance is  $4kT\Delta f/R_p$ , and  $Z_{tank}(j\omega_0) = R_p$ , then Equation 2.14 becomes

$$\overline{i_n^2} = \overline{i_{nR}^2}\left(1 + \frac{\gamma}{\alpha}\right). \quad (2.16)$$

In the quadrature VCO configuration, the new effective  $g_m$ , including the coupling devices and change in regenerative transconductance, is

$$g_{m_{eff}} = g_C + g_Q = g_C(1 + m). \quad (2.17)$$

From Equation 2.11,

$$g_C = \frac{1}{|Z_{tank}(j\omega_1)|\sqrt{1 + m^2}}. \quad (2.18)$$

For  $m = 0.53$ , the magnitude of the tank impedance at  $\omega_1$  is 66% of the magnitude of the tank impedance at  $\omega_0$ . Thus, Equation 2.17 becomes

$$g_{m_{eff}} = g_{C0} \frac{|Z_{tank}(j\omega_0)|}{|Z_{tank}(j\omega_1)|\sqrt{1 + m^2}}(1 + m) = 2.05g_{C0}. \quad (2.19)$$

Using this new transconductance and Equation 2.14, the effective noise current power in quadrature is

$$\overline{i_{nQ}^2} = 2 \left( \overline{i_{nR}^2} \left( 1 + 2.05 \frac{\gamma}{\alpha} \right) \right). \quad (2.20)$$

The factor of two arises because now there are two identical tanks that each contribute to the total noise current power at the output.

The effect of oscillating away from the resonant peak of the tank can be modelled by changing the quality factor  $Q$  in Equation 2.13, as done by van de Ven, et al., in [40]. The quadrature VCO is considered to be a two stage ring oscillator with each stage being a differential core. The quality factor of a closed-loop system has been shown by Razavi in [38] to be

$$Q = \frac{\omega_0}{2} \sqrt{\left(\frac{\partial A}{\partial \omega}\right)^2 + \left(\frac{\partial \phi}{\partial \omega}\right)^2}. \quad (2.21)$$

If  $H(j\omega)$  is the open loop transfer function, then  $A = |H(j\omega)|$  and  $\phi = \angle(H(j\omega))$ . Van de Ven shows that this quality factor can be approximated for an N-stage LC-ring oscillator to be

$$Q_{eff}(\phi_{ztank}) = N \cdot Q_p \cdot \cos(\phi_{ztank}), \quad (2.22)$$

where  $Q_p$  is the quality factor of the tank at resonance. The phase of the tank at  $\omega_1$  for  $m = 0.53$  is  $27.9^\circ$ . Thus, the total phase noise for the quadrature VCO is

$$\mathcal{L}(\Delta\omega) = 10 \log \left( \frac{1}{2} \cdot \frac{\overline{i_n^2}}{i_{sig}^2} \left( \frac{1}{2(2Q_p \cos(\phi_{ztank}))} \frac{\omega_0}{\Delta\omega} \right)^2 \right). \quad (2.23)$$

The worst case phase noise occurs when the noise current is dominated by the active devices (i.e.,  $\gamma/\alpha \gg 1$ ). In this case, the phase noise for the quadrature VCO is only 1.2dB worse than that of the simple VCO core, a minimal increase. Unfortunately, to achieve this small performance degradation, the total power consumed has more than doubled with the addition of the second core and coupling devices.

### 2.3.3 Effect of Mismatch

The above derivation assumes that both cores have identical tank impedances. In reality, some mismatch will occur between the tanks, and this will affect the accuracy of the phase difference between the two cores, moving it away from  $90^\circ$ . To model

this mismatch, the circuit in Figure 2-7 still applies, but now let  $Z_{tank2} = XZ_{tank1}$ . Then Equation 2.6, becomes

$$1 - g_C^2 Z_{tank}^2 (1 + X^2) + 2g_C g_Q^2 Z_{tank}^3 X(1 + X) + g_C^4 Z_{tank}^4 X^2 - g_Q^4 Z_{tank}^4 X^2 = 0, \quad (2.24)$$

or simply

$$1 - G^2(1 + X^2) + 2m^2 G^3 X(1 + X) + (1 - m^4)G^4 X^2 = 0. \quad (2.25)$$

If  $X = 1$ , this degenerates to the previous case, so consider the case where  $X = 1 + \Delta X$ . Then  $G$  becomes some value  $G_0 + \Delta G$ . Assuming that  $\Delta X$  is small enough, then  $\Delta G/\Delta X = \partial G/\partial X$ , and it can be found that

$$\frac{\partial G}{\partial X} = \frac{2G^2 X - 2m^2 G^3 (2X + 1) + (1 - m^4)G^4 2X}{-2G(1 + X^2) + 6m^2 G^2 X(1 + X) + 4(1 - m^4)G^3 X^2}. \quad (2.26)$$

Centering this value around the point when  $X = 1$  and  $G = 1/(1 + jm)$ ,

$$\left. \frac{\partial G}{\partial X} \right|_Q = \frac{4 - 8m^2 - 2m^4 + j(4m - 6m^3)}{24m^2 - 12m^4 + j(-12m + 28m^3 - 4m^5)}. \quad (2.27)$$

Equation 2.9 can be rewritten in terms of  $m$ ,  $G$ , and  $X$  as

$$\begin{aligned} A &= A \\ B &= \frac{-G + m^2 G^2 X + G^3 X^2}{1 - G^2 X^2 + m^2 G^3 X^2} A \\ C &= \frac{mG^2 X^2 + mG^2 X - m^3 G^3 X^2}{1 - G^2 X^2 + m^2 G^3 X^2} A \\ D &= \frac{-mGX - mG^3 X^2}{1 - G^2 X^2 + m^2 G^3 X^2} A \end{aligned} \quad (2.28)$$

The theoretical difference of the phase of the output can be calculated assuming a small  $\Delta X$  as  $C = C_0 + \Delta C = -jA + \Delta C$ , where  $\Delta C = \Delta X(\partial C/\partial X)$ . It can be found that

$$\begin{aligned} \frac{\partial C}{\partial X} &= \frac{mG^2 + 2mG^2 X - 2m^3 G^3 X + mG^4 X^2 - m^3 G^5 X^2}{(1 - G^2 X^2 + m^2 G^3 X^2)^2} \\ &+ \left( \frac{2mG + 2mGX^2 - 3m^3 G^2 X^2 - 2mG^3 X^2 + 2m^3 G^4 X^2 + 2mG^3 X^3 - 3m^3 G^4 X^3}{(1 - G^2 X^2 + m^2 G^3 X^2)^2} \right) \frac{\partial G}{\partial X}. \end{aligned} \quad (2.29)$$

One thing to note from this equation is the effect of  $m$  on this value. As  $m$  gets very small,  $|G| \rightarrow 1$ ,  $\left. \frac{\partial G}{\partial X} \right|_Q \rightarrow \infty$ , and

$$\lim_{m \rightarrow 0} \frac{\partial C}{\partial X} = \lim_{m \rightarrow 0} \frac{4m + 4m \frac{\partial G}{\partial X}}{(1 - G^2)^2} = \lim_{m \rightarrow 0} \frac{4m + 4m \frac{\partial G}{\partial X}}{(jm)^2} = \infty. \quad (2.30)$$

Also, as  $m$  gets large,  $|G| \rightarrow 1/m \rightarrow 0$ ,  $\left| \frac{\partial G}{\partial X} \right|_Q \rightarrow 1/m \rightarrow 0$ , and  $\left| \frac{\partial C}{\partial X} \right| \rightarrow 3.5$ .  $m$  determines the amount of coupling between the two VCO cores, and as would be expected, the stronger the coupling, the smaller the effect of any mismatch between the cores.

Any further symbolic manipulation of Equation 2.29 is rather difficult, but the phase error is

$$\Delta\phi = \tan^{-1}\left(C + \Delta X \frac{\partial C}{\partial X}\right) - 90^\circ. \quad (2.31)$$

This phase error is plotted in Figure 2-9, assuming that  $\Delta X = 0.02$ , which allows up to a 2% mismatch between the passive components of the tanks. The graph shows that when  $m = 1.43$ , the phase error is zero, even though there would still be a difference in magnitude between the I and Q outputs. To achieve this, though, the current through the transistors coupling the core together must be almost one and a half times that through the cross-coupled regenerative transistors. Since the vast majority of the power budget is consumed by the VCO cores and the phase error does not have to be exactly zero, a value of  $m = 0.53$ , is chosen, which should produce a phase error of  $-1.2^\circ$ . The simulated phase error is higher than this prediction because this model assumes a linear response to tank mismatch.

One method to limit the nonlinearities and improve the phase error performance is described in [20], which proposes tying the *ICOM* nodes of both cores together from Figure 2-6, and also tying the *QCOM* nodes of both cores together. The nonlinearities present in the circuit produce a signal on the *ICOM* node that will only contain the even harmonics of the fundamental frequency, so its lowest frequency component will be at twice  $f_0$ , the output frequency of the VCO. Since the second core is phase-shifted by  $90^\circ$ , this is effectively phase shifting the signal at *ICOM* by  $180^\circ$ , since it

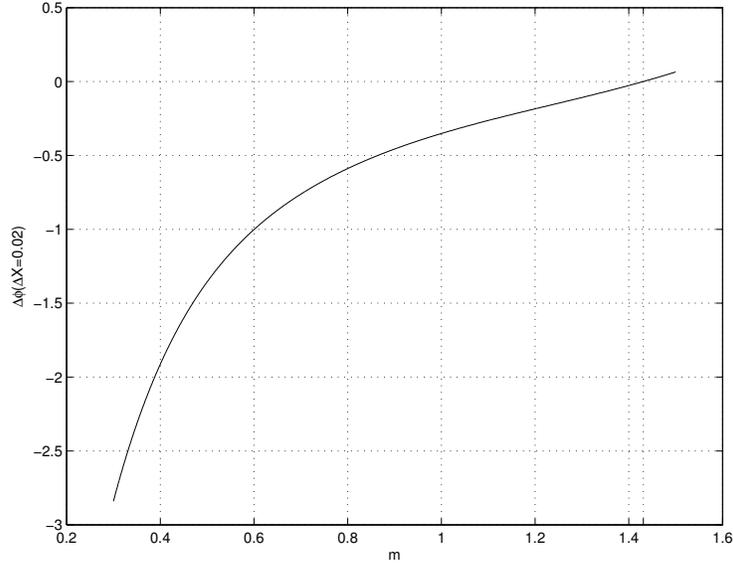


Figure 2-9: Theoretical phase error versus coupling coefficient  $m$  assuming  $\Delta X = 0.02$

is twice the frequency. By connecting the two *ICOM* nodes together, when one core needs to supply more current, the other core will require less current, which should cancel the second harmonic component, making that node closer to a true ground. The same argument applies to the *QCOM* nodes. This VCO uses this technique.

### 2.3.4 First Approach to Force One Mode of Quadrature

One method to force the VCO into the low frequency, stable mode  $M_1$  is to inject the desired phase of the output onto the tank nodes of the *Q* (right) core. To flip the quadrature mode, the output of the second core must be inverted. Thus, by shorting the two nodes  $V_{OQP}$  and  $V_{OQN}$  together, the desired output phase is injected directly on top of the incorrect signal. Since these two phases are inverses of each other, by adding them together the tank turns off. After being shut off for a short period of time, the tank is allowed to restart, and oscillation resumes, hopefully in the correct quadrature mode.

The modification to the *Q* tank is shown in Figure 2-10. The transistor  $M_{N18}$  is turned on by  $V_{SHORT}$ . In order to minimize its on resistance for a given width, this transistor is AC coupled to the tank nodes and has its source and drain set at a



cycle and its inverting output should have a 75% duty cycle. Therefore,  $QBI$  will be lower than  $IBQ$ , so the output of the OTA,  $NERRQ$  will be low, and  $ERRQ$ , which signifies the oscillator is in the wrong quadrature mode, is high.

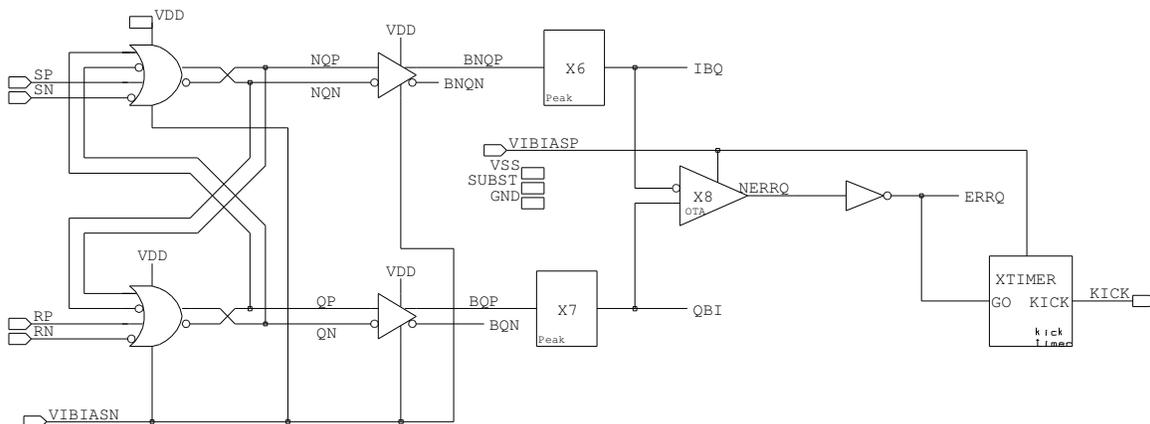


Figure 2-11: Controller circuit that can detect whether the VCO is in the incorrect quadrature mode. The  $I$  outputs of VCO connect to the set input, and the  $Q$  outputs connect to the reset input.

By shorting the second tank out, it effectively turns off, so  $V_{OQP} - V_{OQN} \rightarrow 0$ . To let the  $Q$  tank start up again, it is shorted only for a limited period of time, as set by the timer circuit shown in Figure 2-12.  $KICK$  is connected to  $V_{SHORT}$  of Figure 2-10. If  $GO$  is low, which signifies that the VCO is in the correct quadrature mode, then  $DISCHARGE$  is high,  $SAW$  is low, and  $KICK$  remains low. If instead,  $GO$  is high, then  $M_{P1}$  drives  $20\mu A$  of current into  $C_1$ . Assuming that  $SAW$  starts at ground, it takes  $0.8V \cdot 1pF / 20\mu A = 40ns$  for  $SAW$  to rise above  $V_{CTIME}$  and the output of  $X_6$  to rise. After the propagation delay through the four CMOS inverters,  $t_{p_{CMOS}}$ ,  $KICK$  should also go high. When  $K2$  goes low, though,  $M_{N1}$  will discharge  $C_1$  and lower  $SAW$ . After another  $t_{p_{CMOS}}$ , therefore,  $KICK$  should go low again. The length of the high pulse of  $KICK$  is roughly proportional to  $t_{p_{CMOS}}$ , so  $C_2$  and  $C_3$  can be increased to lengthen the time that  $KICK$  is high.

This approach to force the VCO into the correct quadrature mode unfortunately fails to reliably flip the output of the  $Q$  tank. Since  $M_{N18}$  in Figure 2-10 has a nonzero on resistance, the two tank nodes are not entirely shorted. While the amplitude of the

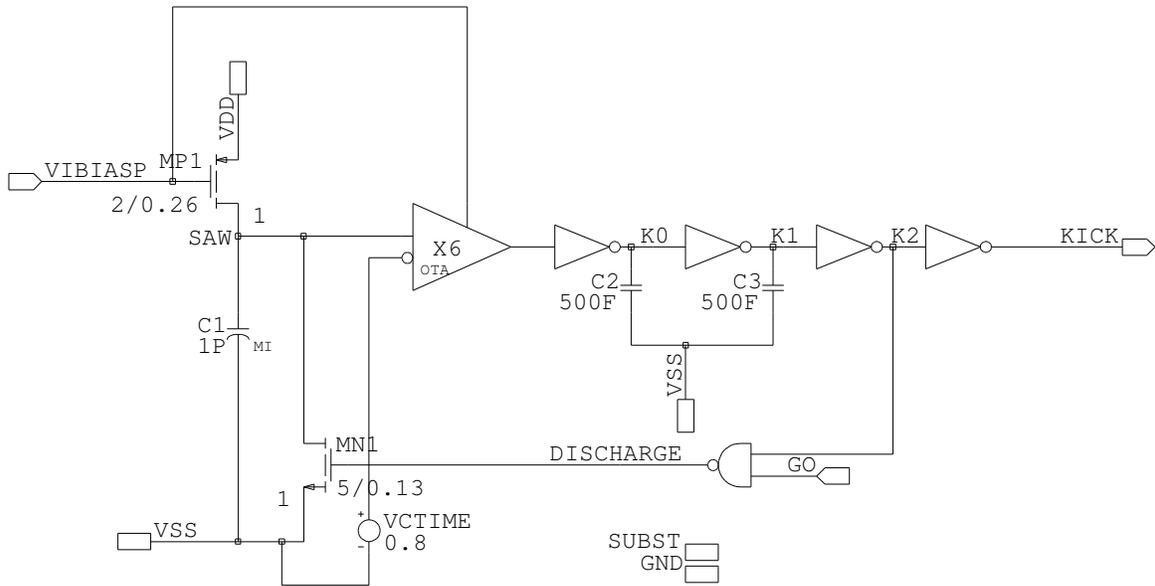


Figure 2-12: Timer circuitry to produce a finite pulse for *KICK*, the control for the shorting transistor in the *Q* core

*Q* tank drops dramatically, the phase does not completely flip around. When  $V_{SHORT}$  returns low, the oscillation then may grow back into the undesired mode of operation. Figure 2-13 shows the output nodes when the VCO is in its eighth capacitor bank and the *Q* core is shorted.  $V_{OI}$  is still ahead of  $V_{OQ}$ , and once the *Q* tank is not shorted,  $V_{OQ}$  remains in the incorrect mode of operation.

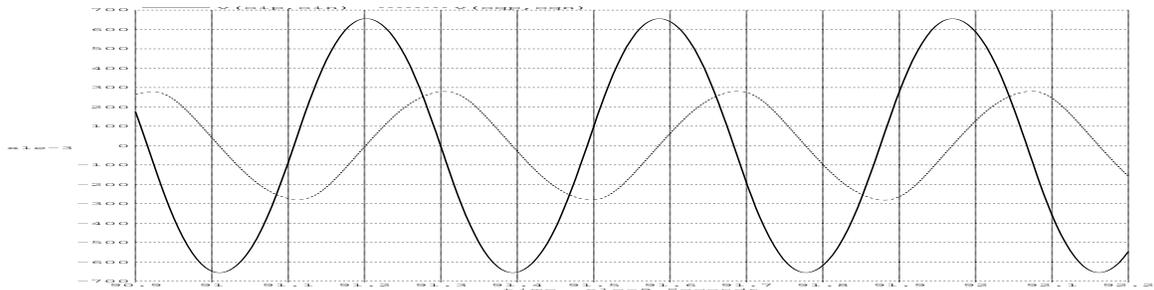


Figure 2-13: Zoom in on VCO output while second tank node is shorted. Note that the  $V_{OQ}$  remains behind  $V_{OI}$  in phase.

### 2.3.5 Revised Approach to Forcing One Mode of Quadrature

An alternative approach to forcing the lower frequency quadrature mode is based on the observation that with a sufficiently high coupling factor  $m$  between the cores, the higher mode of operation is unstable. Rather than making  $m$  very high at all times which can be a large current draw,  $m$  is increased only when the circuit is in the incorrect quadrature mode.

By adding an extra current source to  $QCOM$  that is only turned on when the VCO is in the incorrect quadrature mode,  $g_Q$ , the transconductance of the coupling transistors can be temporarily increased. Figure 2-14 shows the addition of this extra current source,  $M_{N15}$ .

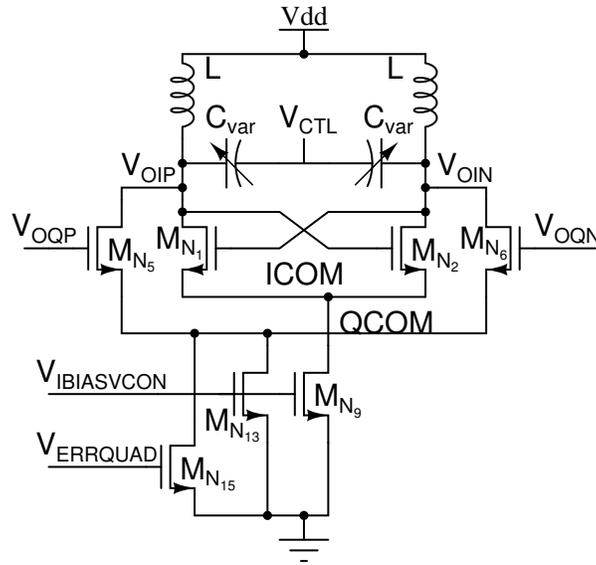


Figure 2-14: Modified VCO core for revised method of forcing quadrature.  $M_{N15}$  is only on when the VCO is in the incorrect quadrature mode

The voltage  $V_{ERRQUAD}$  is derived from the same quadrature error detection circuit of Figure 2-11. The difference is that the timer is no longer used, and  $V_{ERRQUAD}$  is instead connected to  $ERRQ$ . The coupling constant  $m$  is kept high until the circuit reverts to the correct quadrature mode. From simulations, this mode transition happens within 100ns across all banks and operating conditions.

## 2.4 Common mode control loop

The simple VCO core shown in Figure 2-2 produces differential output with a common mode point at  $V_{DD}$ . Since the inductor can produce values greater than the rail, this is not a problem, and assuming proper biasing of any successive buffers, the gate-source voltage of any transistors can be prevented from exceeding 1.2V. The problem with this approach is the limited tuning of the varactors. Since one terminal of the varactor is fixed at the positive supply, the total voltage across the capacitor varies from 0.1 to 1.1V, or -1.1 to -0.1V, depending on which terminal is connected to the control voltage and which to the core. The maximum tuning range of the varactor, however, occurs when the voltage across it is centered around 0V, as seen in Figure 2-15.

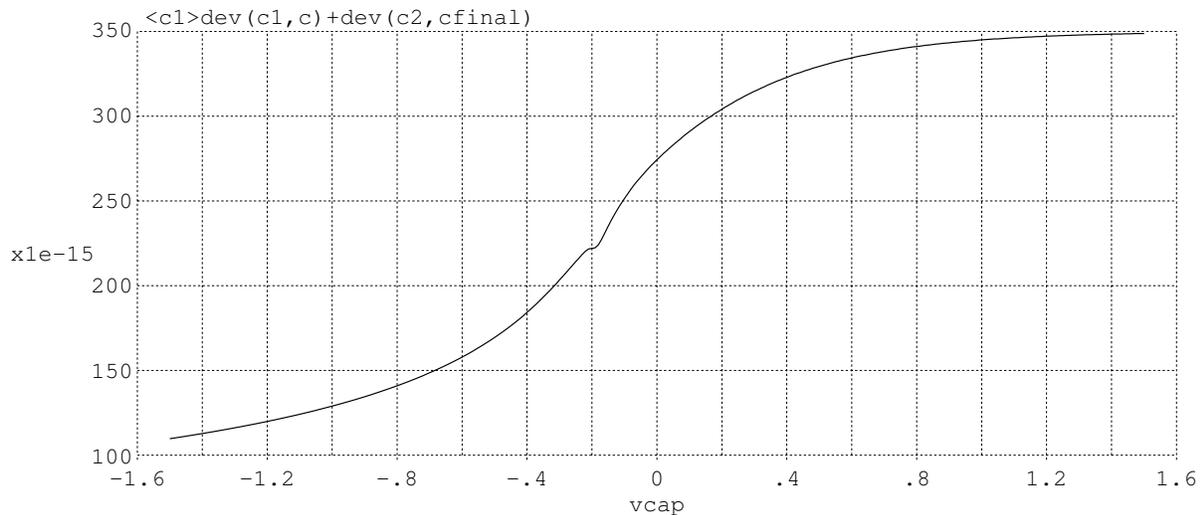


Figure 2-15: Total capacitance of 350fF varactor versus DC bias across it

Maximizing the tunability of the varactor is especially important at the highest frequencies of operation, since only one varactor is switched in. To maximize the highest possible frequency, the varactor must be small, but as more banks are turned on, there must be adequate tuning range for reasonable overlap between banks. Switching in very small capacitors is one solution to the overlap problem, but matching capacitors between the two cores is more difficult as the capacitors get smaller. As was shown above in Section 2.3, the phase accuracy of the output is highly dependent

on the match of the two tank impedances. In addition, as the size of the capacitors is decreased, the digital control circuitry for coarse tuning increases in complexity and requires more time to find the correct bank. Thus, high tuning range for a given varactor is beneficial, and the common mode voltage of the core's output is reduced from 1.2V. To keep the active devices in saturation, this voltage is set at 0.65V.

To set the common mode voltage, a variable resistor implemented as a PMOS transistor is placed in series with the two inductors in each core, as shown in Figure 2-16. The top terminal of the inductors  $V_{TAPCM}$  is a differential AC ground and is the common mode DC potential of the output. The voltage at this point is compared to a reference voltage,  $V_{REFCM}$ , produced by a cascode current source driving  $R_{CM}$ . The amplified difference between these two signals is then fed back to adjust the gate of the pullup transistor. If the common mode voltage is too high,  $V_{CMCTL}$  rises,  $M_{PU}$  has a higher drain/source impedance, and the common mode voltage drops.

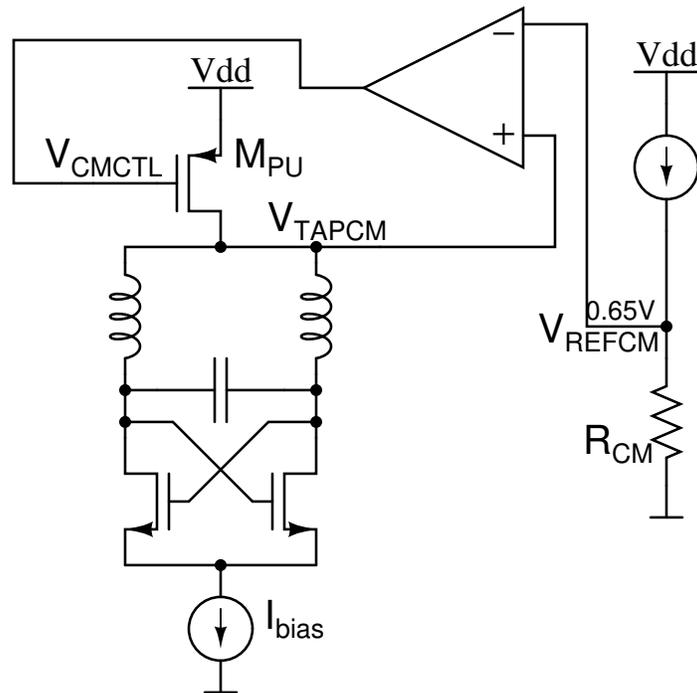


Figure 2-16: Common mode control schematic showing placement of variable resistor for common mode control

As will be described in Section 2.5, the current draw increases greatly, by almost

a factor of four, as more capacitor banks are added and the frequency drops. To keep relatively constant common mode control loop dynamics, additional transistors are switched in at lower frequencies, as shown in Figure 2-17, so that the devices can handle all the current. Each of these extra pullup devices is switched in along with one of the capacitor banks. Since the banks are switched in thermometer-style, that means these extra pullups are also switched in thermometer-style; however, an extra pullup device is not switched in with every bank. In the final design, these pullup devices are switched in with  $C_3$ ,  $C_6$ ,  $C_9$ , and  $C_{15}$ .

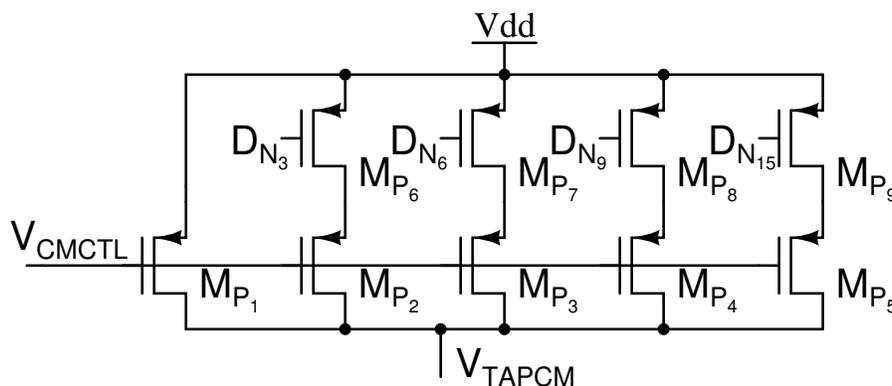


Figure 2-17: Actual implementation of pullup transistor of Figure 2-16.  $D_{N_i}$  is active low when capacitor bank  $i$  is switched in

Since there are two cores, rather than having separate common mode control loops, only one is used. This has the advantage that two transconductance amplifiers do not need to be well matched, but any differences in the pullup network of the two cores is reflected in phase error on the output. The common mode points of the two cores are averaged before the OTA.

The linearized model of the common mode control loop is shown in Figure 2-18. The control loop has two poles, one from the pullup resistor, and one from the OTA, which is described in Section 2.6. The impedance of the pullup resistor is very small since the transistor is in the linear region of operation. The effective resistance can be calculated by noting the 0.55V is across the resistor when the current through it is 4mA, which occurs at the highest frequency bank, so  $R_{PU} = 137.5\Omega$ . The oscillator operates at 3.2GHz in the top frequency bank, and the total inductance,

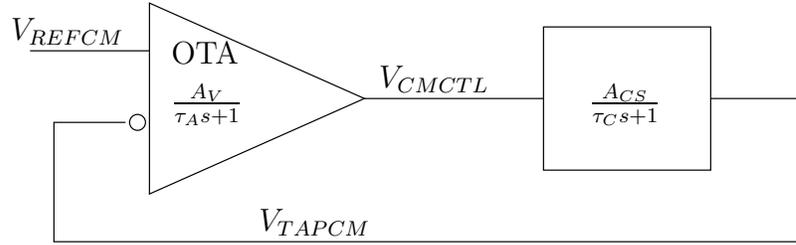


Figure 2-18: Common mode control loop block diagram

as will be mentioned in Chapter 4, is 1.15nH, so the approximate capacitance on one of the output nodes is 2.0pF. This neglects the result described above that the quadrature loop causes the frequency to be lower than the resonant frequency of the tank, so this 2.0pF is a conservative estimate. The common mode loop actually sees twice this capacitance because it drives both of the differential output nodes of the VCO core. Therefore, the pole from the pullup resistor and the VCO core is  $p_1 = 1/(2\pi\tau_C) = 289\text{MHz}$ . At lower frequencies, the total capacitance goes up by a factor of four, but the current draw of the cores also goes up by a factor of four, so the on resistance is quartered, keeping the pole in roughly the same location. Because  $M_{PU}$  is in the linear region, it has very small gain, and  $A_{CS}$ , the DC gain of the pullup resistor from  $V_{CMCTL}$  to the output common mode voltage, can be derived from simulations as 0.5.

The OTA is the dominant pole in the loop, so it must be chosen to provide adequate phase margin for the loop. The simulated DC gain of the loop is 18.3dB, or 8.24. Thus, by setting the dominant pole at  $p_1/8.24 = 35.1\text{MHz}$ , a phase margin of  $45^\circ$  is achieved. By compensating the OTA with a 100fF capacitor, the actual first pole is at 32.0MHz, giving a slightly greater than  $45^\circ$  phase margin and ensuring adequate stability of the loop.

## 2.5 Amplitude control loop

The simple VCO core presented at the beginning of the chapter is designed to have a gain of greater than one at low oscillation amplitudes. As the oscillation amplitude

increases, the average  $g_m$  of the active devices decreases, until the total loop gain is precisely equal to one, leading to stable amplitude oscillations. The amplitude on the output is highly dependent therefore on any process and temperature variations that affect the  $g_m$  of  $M_1$  and  $M_2$ . In particular, at higher temperatures, as the mobility of electrons decreases, the oscillation amplitude drops. In addition, the startup gain of the VCO also decreases. To ensure an adequate startup gain across all temperature and process variations, the devices must be made very wide, or the bias current must be increased. The former approach increases the total amount of fixed capacitance on the tank nodes, whereas the second approach uses excess power at all but the worst operating conditions.

Another approach is to dynamically control the bias current, increasing the current when the VCO output has a small amplitude. An active amplitude control loop is used in this thesis because it can ensure startup and constant oscillation amplitude over a large range of conditions while conserving power through the core when not in the absolute worst conditions. As shown in Figure 2-1, a peak detector is connected to the output of the VCO, which senses the amplitude of oscillation. This is then compared to a reference voltage and used to set the bias current through the VCO cores. When the output has a small oscillation amplitude, such as at startup, this loop adds more current to the core node until the target amplitude is reached.

### 2.5.1 Peak Detector

A very simple peak detector is used in this circuit, since it requires little current, and works adequately over any process variations. The peak detector is shown in Figure 2-19. To understand its operation, consider a sinusoidal input to  $V_{I1}$ . The circuit, in small signal, looks like a source follower. With a sufficiently large  $C_1$ , the input is at a much higher frequency than the first pole ( $p_1 = C_1/g_m$ ), and the high frequency signal is greatly attenuated.

The bias point of the output is dependent on the amplitude of the signal. As Figure 2-20 shows, the input rises above  $V_O + V_{tp}$  for part of the period, turning off the transistor. Then the DC voltage of the output is the point where the current

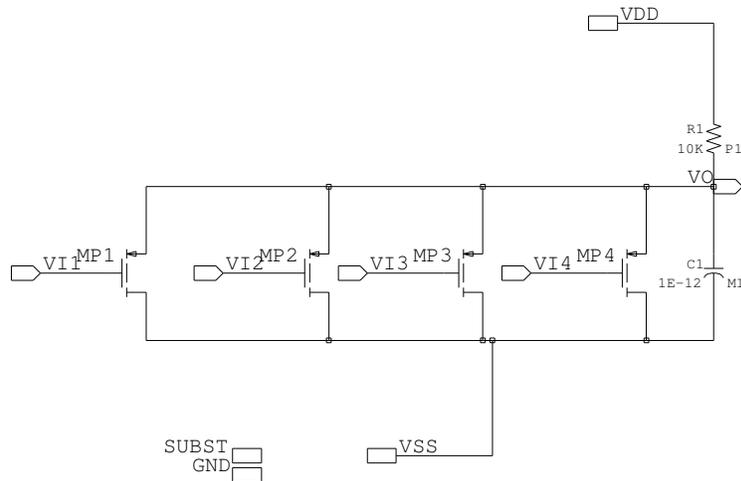


Figure 2-19: Peak detector schematic

through the transistor, when on, is enough to counter the current that is constantly being supplied through  $R_1$ .

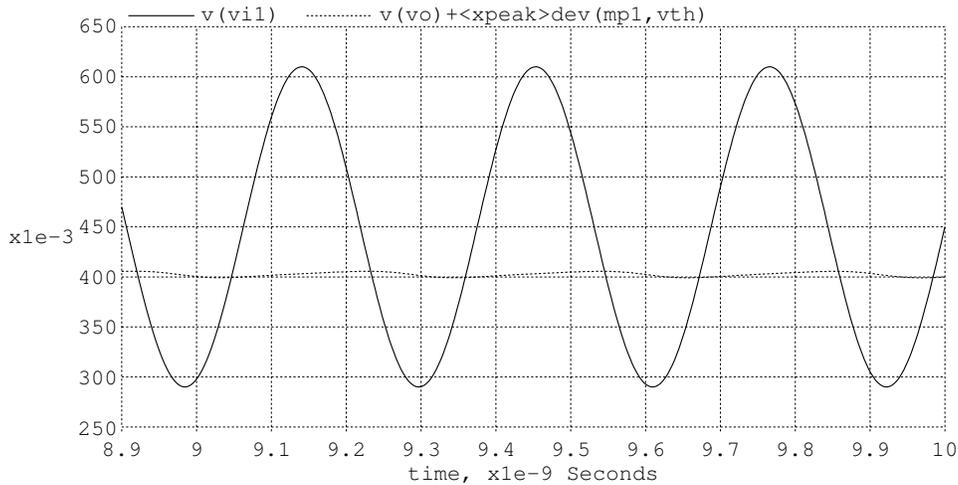


Figure 2-20: Steady-state operation of the peak detector with a 1.6GHz input wave. The output is shifted by  $V_{tp}$ , the threshold voltage

All four VCO tank nodes are connected to the peak detector to minimize ripple. The output of the peak detector is  $v_O = V_O + v_o$ . The magnitude of this ripple is  $v_{opp} \approx (V_{DD} - V_O)\delta_p/RC$ , where  $\delta_p$  is the length of the time that the transistor is off. By connecting all four nodes to the peak detector, the interval  $\delta_p$  is quartered, which reduces the ripple by four.

The peak detector's response to a change in amplitude is asymmetric. Consider first a step drop in the amplitude, which turns off all the transistors. Then the peak detector's output rises according to the time constant  $1/(R_1C_1)$ . Inversely, suppose the amplitude of the oscillator suddenly increases. If the transistor is large enough, then at the next peak on the input, the peak detector's output drops to the correct value. Thus, in discharging the capacitor, the peak detector acts as a zero order hold function, sampling the VCO output at its peaks.

## 2.5.2 Loop Dynamics

Modeling the amplitude control loop is more difficult than modeling the common mode control loop because it depends heavily on the nonlinearities of the peak detector. The linearized model of the amplitude control loop is shown in Figure 2-21.

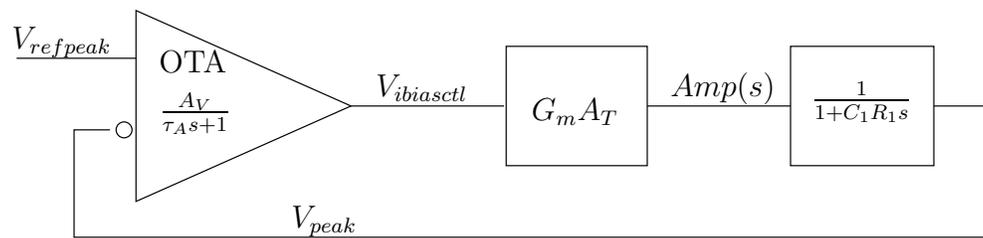


Figure 2-21: Amplitude control loop block diagram

The amplifier used to compare the reference voltage to the sensed amplitude is an operational transconductance amplifier, described in Section 2.6, with approximate transfer function  $H(s) = A_V/(1 + \tau_A s)$ . Its output is passed into a bias network which generates, with transconductance  $G_m$ , a current through the core, but then the current is converted to an amplitude in a nonlinear fashion. For any given bias current, the steady-state amplitude corresponds to the amplitude at which the  $g_m$  of the cross-coupled transistors in the core is the inverse of the lumped parasitic resistance of the tank. Assuming small changes in current, this current to amplitude conversion can be modelled as a simple gain  $A_T$ . Then, finally, the peak detector converts this amplitude into a voltage. Since the response of the peak detector to a

step increase in amplitude is at most a delay of one output period, it operates well above the loop bandwidth and can essentially be ignored; therefore, only the peak detector's response to a step decrease in amplitude affects the loop dynamics. It is modelled as a unity gain low pass filter with a pole at  $\omega = 1/(R_1C_1)$ . The total open-loop transfer function is

$$L(s) = \frac{G_m A_T A_V}{(1 + \tau_A s)(1 + R_1 C_1 s)}. \quad (2.32)$$

Since the peak detector's pole is not fixed and can move to much higher frequencies, the OTA's pole is made the dominant one. The gain from  $V_{biasctl}$  to the amplitude of the signal is extracted from simulations as  $G_m A_T = (0.011)(310) = 3.4$ . From Section 2.6,  $A_V = 16.2$ . This means that for a phase margin of  $45^\circ$ , the dominant pole must be near  $1/(R_1 C_1 G_m A_T A_V) = 1.82 \text{Mrad/s}$ . By setting the compensation capacitor in the OTA to be 15pF, this yields  $\tau_A = 5.5 \times 10^{-7} = 1/(1.8 \text{Mrad/s})$ . In simulations, however, this compensation scheme is highly conservative, especially considering that for any increase in amplitude the peak detector reacts extremely quickly. The final compensation capacitor in the OTA is set to 2.5pF, which places its pole at 11Mrad/s and produces good settling characteristics in simulation.

### 2.5.3 Interaction With Common Mode Control Loop

As the amplitude control loop increases the current through the VCO core, the common mode voltage drops if the pullup impedance remains constant. As the common mode voltage drops, though, the minimum point of the core output also drops, which causes the peak detector to sense a larger amplitude because it detects the minimum point on the output, even if the peak-to-peak amplitude has not grown. This could lead to possible instability and must be accounted for in the design of the two loops.

Two interactions between the loops occur. The output voltage of the tank is AC coupled into the peak detector. Thus, any change in the common mode point, after passing through the high pass filter of the AC coupling, is added to the input of the peak detector. Any change in the current through the core nodes, as set by the

amplitude control loop, is converted into a change in the common mode point of the output as scaled by the resistance of the pullup device. Figure 2-22 shows the linear model, including the above two interactions, of the amplitude and common mode control loops.

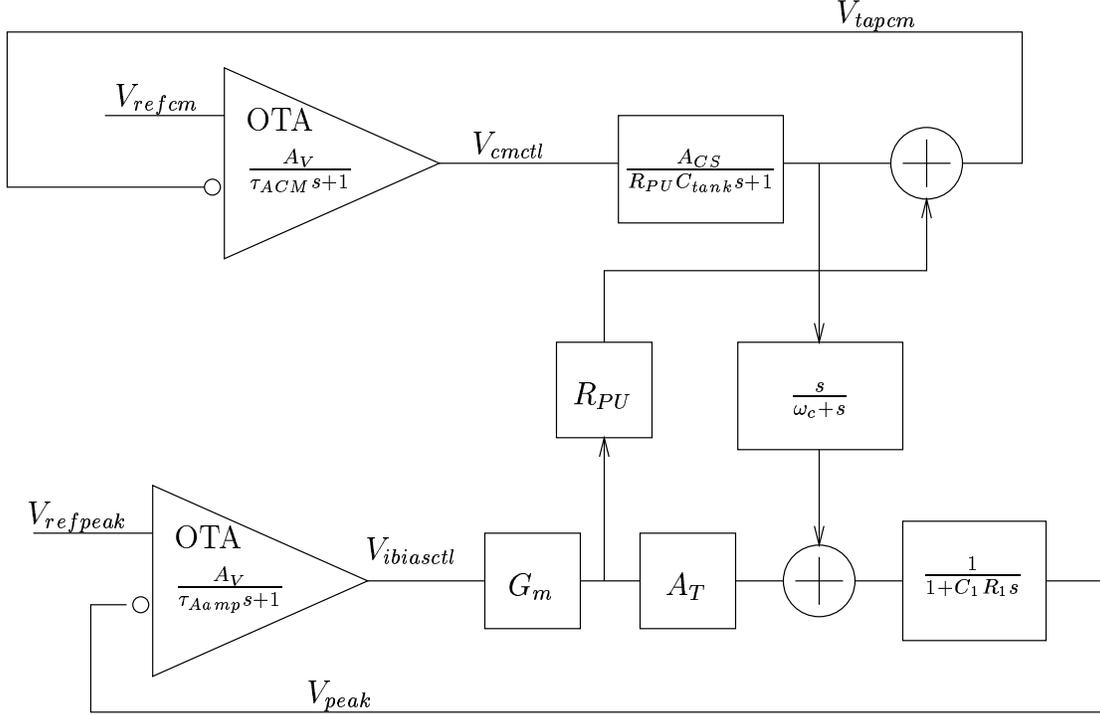


Figure 2-22: Linear model containing both the amplitude and common mode loops and the interactions between them

This figure shows that another loop exists which has the potential for instability. This third loop has the open loop transfer function

$$L_{inter}(s) = \frac{A_V^2 A_{CS} G_m R_{PU} s}{(\tau_{ACM} s + 1)(R_{PU} C_{tank} s + 1)(s + \omega_C)\left(\frac{R_1 C_1}{s} + 1\right)(\tau_{Aamp} s + 1)}. \quad (2.33)$$

The only real control available that does not affect the dynamics of the principal two loops is to choose a value for  $\omega_C$ , the pole in the AC coupling of the VCO output to the peak detector input. This pole must be sufficiently low in frequency that this AC coupling looks like a short at the lowest operating frequency of the VCO, 1.6GHz. By setting  $\omega_C$  to be 440 Mrad/s, the resultant open loop transfer function

is as shown in Figure 2-23, which yields a phase margin of  $30^\circ$ . This means that the interaction is still stable, though some peaking may occur, but once again this assumes the most conservative pole location for the peak detector. In simulations, the interaction between the loops produces no ringing on the output, confirming that this third loop is stable.

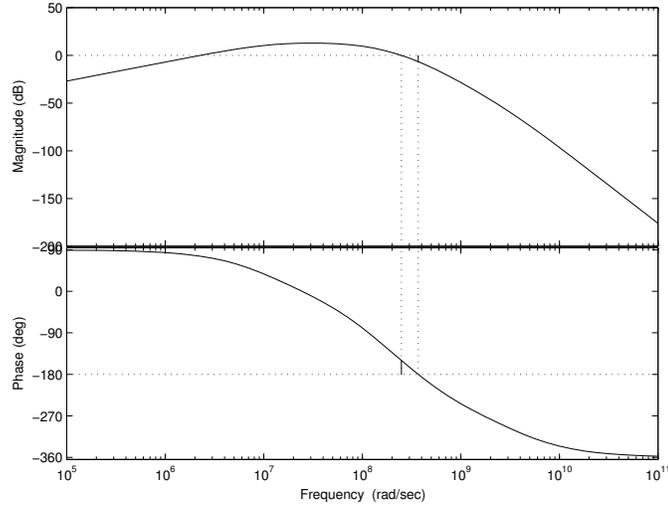


Figure 2-23: Bode plot of  $L_{inter}(s)$ , the third loop created from interactions between the amplitude and common mode control loops. Phase margin is  $30^\circ$ , and gain margin is 6.54dB.

## 2.6 Operational Transconductance Amplifier

An operational transconductance amplifier (OTA) acts as an error amplifier and provides gain in both the common mode and amplitude control loops. The circuit topology in both of these loops is identical; only the value of the compensation capacitor is changed. The OTA circuit schematic is shown in Figure 2-24. The circuit includes a single gain stage which has a DC gain of  $g_{m_{p10}} \frac{g_{m_{n30}}}{g_{m_{n28}}} R_o = 10g_{m_{p10}} R_o$ . The factor of ten comes in because  $M_{P13}$  has 10 times as much current and is ten times wider than  $M_{P12}$ , so it has ten times the transconductance since  $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$ .

The compensation capacitors are placed around the output transistors to mini-

mum their size. This also has the effect of moving the dominant pole to node  $V_{X1}$  and  $V_{X2}$ . To see the advantage of this, first note that if  $C_{COMP}$  was connected between the output and ground, the first pole location would be  $p_1 = 1/(R_o C_{COMP})$ . With the compensation capacitor connected in feedback around the last stage, the Miller effect causes the effective capacitance on node  $V_{X1}$  to be  $C_{eff} = (1 - A_V)C_{COMP} = (1 + g_{m_{p13}}R_o)C_{COMP}$ . The effective resistance seen at  $V_{X1}$  is  $1/g_{m_{p12}}$ , so the pole location is at  $p'_1 = g_{m_{p13}}/((1 + g_{m_{p13}}R_o)C_{COMP}) \approx 1/(10R_o C_{COMP})$ . Thus, for the same size capacitor, the dominant pole is at one-tenth the frequency.

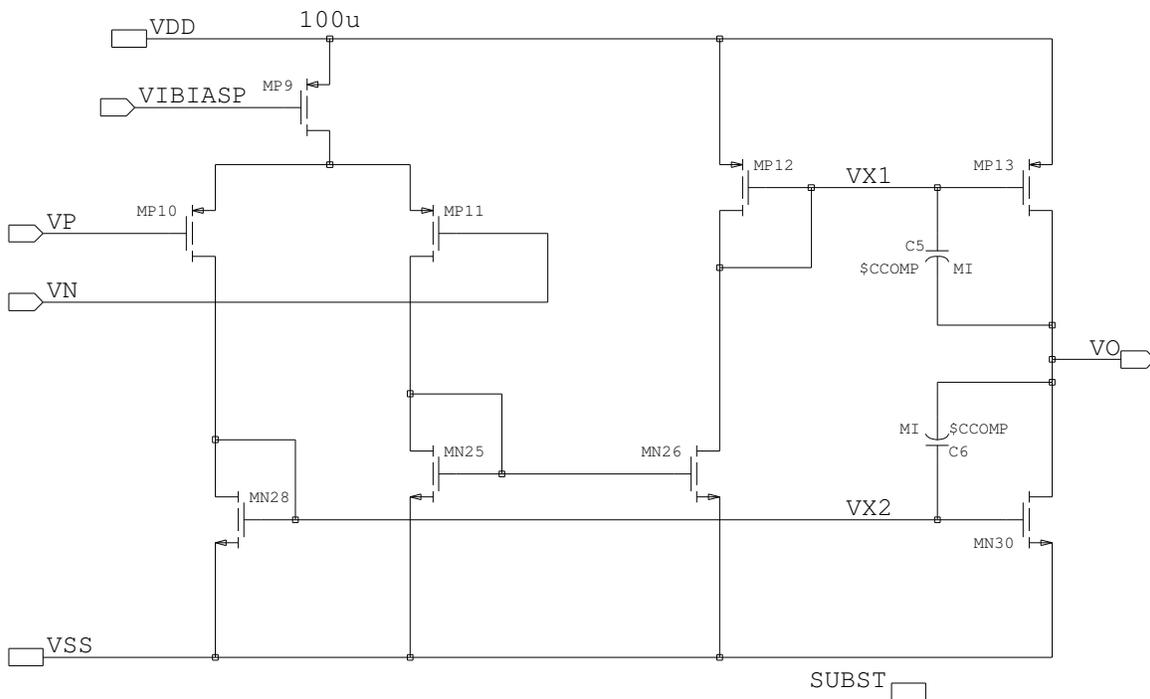


Figure 2-24: Operational transconductance amplifier schematic

The actual effect of the various compensation capacitors can be seen in Figure 2-25, which shows the simulated frequency response of the operational transconductance amplifier with various values of  $C_L$ . As is shown, the DC gain is 24.3dB, and the dominant pole can vary from 147MHz with no compensation to 882kHz if  $C_{COMP} = 5\text{pF}$ . The actual value of the compensation is chosen to suit the dynamics of the specific control loop, as described earlier in this chapter.

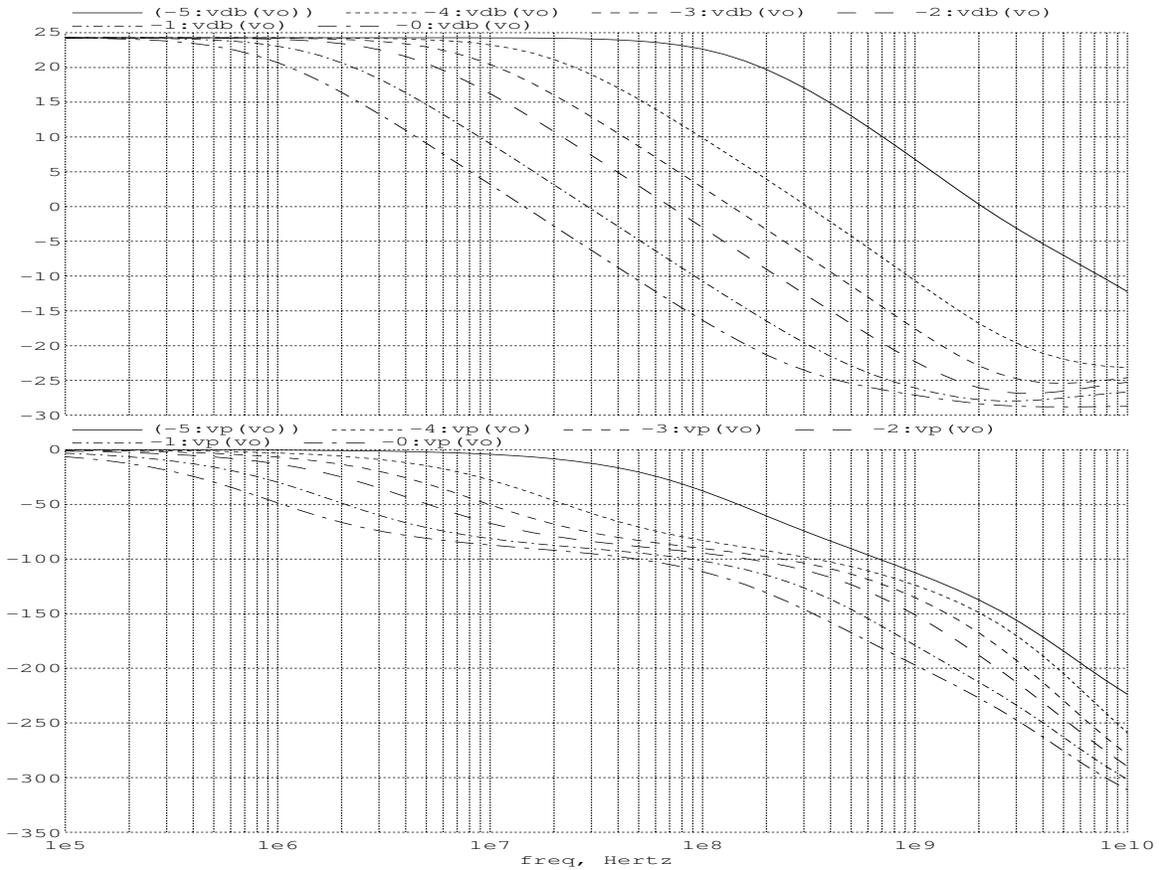


Figure 2-25: Simulated frequency response of operational transconductance amplifier for values of  $C_{COMP} = 0, 200\text{fF}, 500\text{fF}, 1\text{pF}, 2.5\text{pF}, 5\text{pF}$

## 2.7 Summary

The VCO design is difficult because it is dependent on nonlinearities, such as the quadrature phase response to tank mismatch and the settling of the amplitude of the oscillator. Many linear approximations were made in the design, with simulations being used to adjust the calculated component values as needed. The final design is included in the appendix in Figure A-1.

Many of the design choices described above modify the simple core in order to make the VCO more robust. The amplitude control loop causes a high startup gain across process and temperature variations. The common mode control loop is used to increase the overlap between capacitor banks, so if two successive banks have mismatched capacitors, there will not be an uncovered region within the total tuning

range. The quadrature mode forcing subcircuit makes the VCO switch to the stable quadrature mode reliably and quickly.

To extend the frequency, a set of 22 capacitor banks is used as the variable capacitance in the tank node. The banks are switched in sequentially, with the number of active banks monotonically increasing as the VCO goes lower in frequency. The switches themselves are designed to have low impedance but with sufficiently small parasitic capacitance that the maximum frequency of 3.2GHz can still be reached.

The next chapter discusses the design of the rest of the PLL. Of particular relevance for the PLL design is the gain variation discussed in Section 2.2. One advantage of designing both the PLL and VCO is that problems in one can be compensated for in the other.

# Chapter 3

## Phase-Locked Loop Design

The design of the remainder of the components in the PLL is discussed in this chapter. First, the overall PLL loop design is discussed, along with the loop filter implementation. Section 3.2 presents the design of the phase-frequency detector and the digital logic used in its implementation. Section 3.3 explains the charge pump, including the method to compensate for the variation of the VCO gain over frequency. Section 3.4 and 3.5 present the divider and control voltage buffer, respectively. The last section summarizes the design considerations of the PLL.

### 3.1 Loop Design

The general PLL topology is seen in Figure 3-1. The reference clock is compared to a divided down version of the output clock using a phase frequency detector. The PFD produces up and down signals telling the charge pump whether to add or remove charge from the loop filter. The filtered version of  $V_{CTL}$  then is input to the voltage-controlled oscillator (VCO), whose output frequency varies directly with  $V_{CTL}$ .

Since the control voltage needs to vary over a large range to get sufficient tuning in each bank to ensure overlap, a Type II PLL is used, meaning that the loop filter  $H(s)$  includes an integrator. The standard second order filter topology shown in Figure 3-2 has an integrator, but also introduces a zero in the open loop transfer function to stabilize the loop.  $C_{HOP}$  introduces a pole above the crossover frequency of the PLL

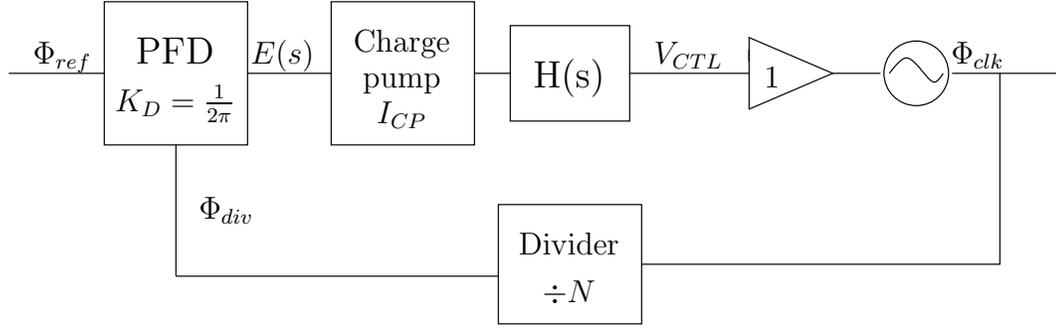


Figure 3-1: Overall PLL block diagram

that filters out some of the high frequency ripple of  $V_{CTL}$ . The loop filter transfer function is

$$H(s) = \frac{v_{CTL}}{i_{IN}}(s) = \frac{R_{PLL}C_{PLL}s + 1}{s((C_{HOP} + C_{PLL}) + sC_{HOP}C_{PLL}R_{PLL})} \quad (3.1)$$

The value of the control voltage is then buffered by a unity gain amplifier to be able to drive the large amount of variable capacitance in the banks of capacitors in the VCO. The pole of this buffer is sufficiently high that it can be simply modelled as an ideal buffer.

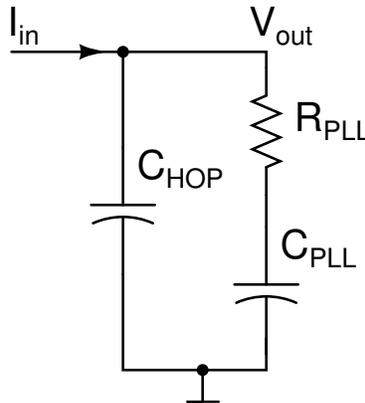


Figure 3-2: Loop filter schematic

The VCO produces an output signal  $V_{CLK} = A\cos(2\pi K_{VCO}V_{CTL}t + \phi_0)$ . The loop

operation only depends on the phase of this output. The VCO's output phase is

$$\Phi_{clk}(t) = \int_{-\infty}^t 2\pi K_{VCO} V_{CTL}(\tau) d\tau, \quad \frac{\Phi_{clk}(s)}{V_{CTL}(s)} = \frac{2\pi K_{VCO}}{s}. \quad (3.2)$$

The actual value of  $K_{VCO}$  varies depending on which bank is selected digitally, and this will be compensated for in the charge pump.

The phase-frequency detector, as explained in Section 3.2, has a gain of  $1/(2\pi)$ . The charge pump produces an average current on its output whose value is  $I_{CP}$  times the average of the error signal. The divider divides both the frequency and the phase (since it is simply the integral of frequency) by  $N$ . In addition, the divider's response to a change in phase on its input is not instantaneous. It is a circuit that only transmits information on a rising edge of its output. The divider, therefore, functions as a zero-order hold circuit whose impulse response is

$$H_{div}(s) = \frac{1 - e^{-s\tau_{ref}}}{s\tau_{ref}}, \quad (3.3)$$

where  $2\pi/\tau_{ref}$  is the reference clock frequency [49]. For frequencies much lower than the reference frequency, this term has approximately unity gain and the same phase as an ideal delay of  $\tau_{ref}$ . Combining all of these, the total open loop transfer function of the PLL is

$$L(s) = \frac{I_{CP}K_{VCO}}{N(C_{HOP} + C_{PLL})} \cdot \frac{1 + R_{PLL}C_{PLL}s}{s^2(1 + s\frac{C_{HOP}C_{PLL}R_{PLL}}{C_{HOP} + C_{PLL}})} \cdot \frac{1 - e^{-s\tau_{ref}}}{s\tau_{ref}}. \quad (3.4)$$

## 3.2 Phase-Frequency Detector

A conventional phase detector, such as the XOR detector, is not suitable for this loop because the output frequency can vary by a factor of more than two and the XOR can lock to higher harmonics of the reference signal. Instead, a modified tristate phase-frequency detector is used, which only locks at the fundamental frequencies of its two inputs. It produces up or down pulses, indicating, respectively, whether  $V_{div}$ , the output of the divider, has a rising edge after, or before, the reference clock

$V_{ref}$ . The average of the difference between the up and down pulses is the phase error between the two clocks. A simplified schematic of the PFD is shown in Figure 3-3, and the full schematic can be seen in Figure A-2. All of the signalling is differential, and the digital logic is implemented using the current mode logic described below.  $R_1$  and  $R_2$  are resettable registers that produce a 1 on the Q output on any rising edges of  $V_{ref}$  or  $V_{div}$ , respectively. Once both  $UP$  and  $DN$  are high, the set/reset latch  $L_1$  resets both registers.  $RST$  stays high until both of the registers' outputs have gone low again.

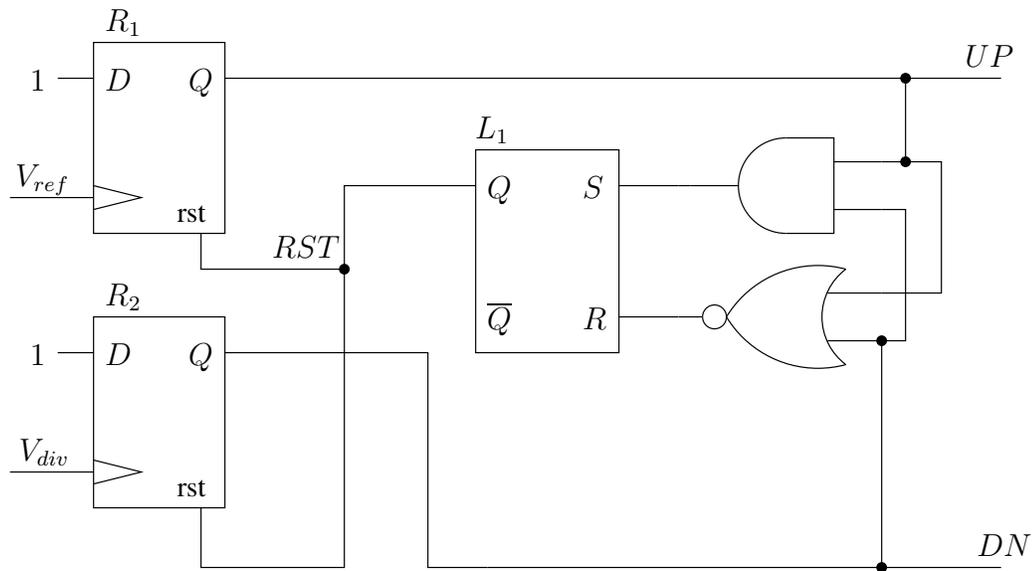


Figure 3-3: Simplified phase-frequency detector schematic

The difference between this and the standard tristate PFD is the addition of  $L_1$  and the NOR gate. If a simple AND gate is used to produce the reset signal, there needs to be sufficient delay in the reset feedback path such that  $RST$  stays high long enough to satisfy the hold times of the registers. The latch and NOR gate simply provide this delay to ensure that both registers reset properly.

The actual values of  $UP$  and  $DN$  have binary amplitudes. When  $UP$  is high, the charge pump adds charge to the loop filter, and when  $DN$  is high, the charge pump removes charge from the loop filter, so  $UP$  and  $DN$  each only take values of 1 or 0. The error signal of the PLL is the average of  $UP - DN$ , and, therefore, this error

signal can vary from  $-1$  to  $1$ . When  $\phi_{REF} = \phi_{DIV}$ , the output is  $0$ , and if  $\phi_{REF}$  is ahead of  $\phi_{CLK}$ , the duty cycle of the  $UP$  pulse will grow until  $UP - DN = 1$  when  $\phi_{REF} - \phi_{CLK} = 2\pi$ . The output of the PFD, therefore, is  $e(s) = (\phi_{REF} - \phi_{DIV})/(2\pi)$ . The transfer characteristic of the PFD is shown in Figure 3-4.

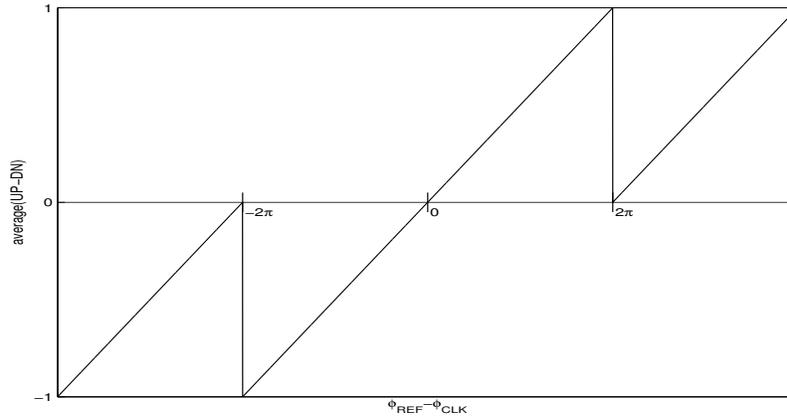


Figure 3-4: Phase-frequency detector transfer curve, showing that its gain is  $1/(2\pi)$

### 3.2.1 Current-Mode Logic

The family of digital logic used in the PLL is differential current-mode logic (CML), also known as source-coupled logic. This logic family is entirely differential and provides two major benefits over other logic families, such as static or dynamic CMOS or DCVSL. The first is that it can be used at very high speeds because only NMOS devices are used, which have a higher current drive capacity for a given width and parasitic capacitance. The second advantage is a noise advantage because the current through the gates is relatively constant, even when the differential output is switching, leading to less noise on both the power supply and the substrate [50]. The other logic families mentioned above all have a much higher variance in their current draw. The biggest disadvantage of CML is its static current, but in this application the limited numbers of CML gates and the high current draw of the VCO make the CML gates only minor contributors to the power consumption.





The up path has two differential stages in order to have a closer propagation delay to the down path that has the extra current mirror of  $M_{P7}$  and  $M_{P9}$ . PFET devices on the input of the down path would eliminate the need for this current mirror, but the outputs of the PFD have a common mode voltage near the positive supply, so they would need to be buffered, which would add extra delay.  $M_{P6}$  and  $M_{N10}$  help force  $M_{P5}$  and  $M_{N12}$  off when  $UP$  or  $DN$ , respectively, is low. It is important to fully turn off the output transistors because any leakage current through them causes more ripple of  $V_{CTL}$ .

### 3.3.1 Compensation for Variation in VCO Gain

The previous chapter mentions that the VCO has a higher gain in the lower frequency banks, since the total amount of variable capacitance is higher when more of the banks are activated. To understand how this affects the overall loop dynamics, the PLL is approximated as a second order system, ignoring the divider delay term and the pole at  $R_{PLL}(C_{HOP} \parallel C_{PLL})$  in Equation 3.4 (i.e.,  $C_{HOP} \ll C_{PLL}$ ). The VCO output frequency is considered fixed. Thus, a change in  $N$  changes the reference frequency. The approximate closed loop PLL system function is

$$G(s) = \frac{NL(s)}{1 + L(s)} = \frac{I_{CP}K_{VCO}}{C_{PLL}} \cdot \frac{1 + \tau_Z s}{s^2 + \frac{\tau_Z I_{CP} K_{VCO}}{N C_{PLL}} s + \frac{I_{CP} K_{VCO}}{N C_{PLL}}}, \quad (3.5)$$

where  $\tau_Z = C_{PLL} R_{PLL}$ . Fitting this to the standard second order form

$$G(s) = \frac{A(1 + \tau_Z s)}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \quad (3.6)$$

yields

$$\omega_n = \sqrt{\frac{I_{CP} K_{VCO}}{N C_{PLL}}}, \quad \zeta = \frac{R_{PLL}}{2} \sqrt{\frac{I_{CP} K_{VCO} C_{PLL}}{N}}. \quad (3.7)$$

The above equations show that the loop dynamics are affected only by the product of  $I_{CP}$  and  $K_{VCO}$ , and as long as that product is constant across frequency banks, the overall frequency response of the PLL should not change. Since  $K_{VCO}$  varies by a factor of four across all the banks, the charge pump is designed to change its current

output, reducing it by a factor of four at lower frequencies.

The circuit in Figure 3-7 is the implementation of the ideal current source of Figure 3-6, which allows the charge pump to compensate for the  $K_{VCO}$  variation. The signals  $D_{P_1}$ ,  $D_{P_2}$ , and  $D_{P_5}$  are active high when the first, second, and fifth banks, respectively, are activated, so if only the highest frequency bank is activated,  $D_{P_1} = D_{P_2} = D_{P_5} = 0$ , turning on switches  $M_{P_{16}} - M_{P_{18}}$ , putting  $200\mu A$  through  $M_{N_{26}}$ . Therefore, at the highest frequency bank,  $I_{CP} = 200\mu A$ . Inversely, at the lowest frequency bank, the three switches are turned off, so  $I_{CP} = 50\mu A$ . These values are chosen so that  $I_{CP}K_{VCO} \approx 22500 A \cdot \text{Hz}/V$  over the entire frequency range.

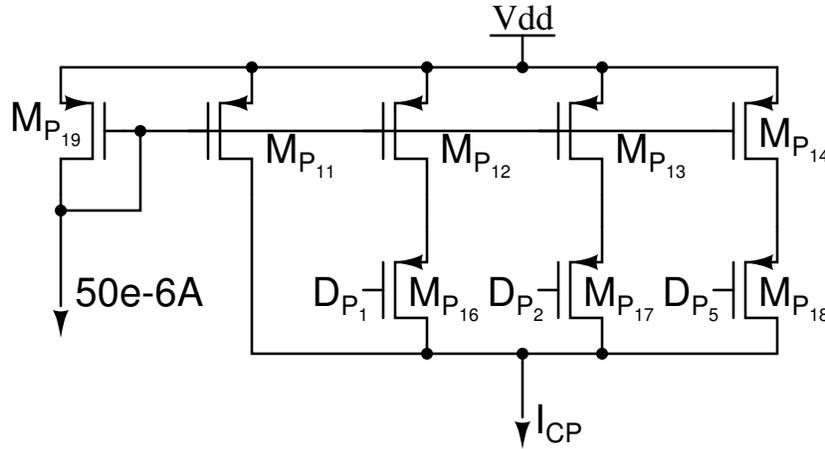


Figure 3-7: Implementation of the current source in the charge pump. This circuit produces a charge pump current that is roughly inversely proportional to  $K_{VCO}$ , the gain of the VCO

### 3.3.2 Loop Filter Design

To determine the overall loop dynamics, the loop filter values must be chosen. The lowest reference frequency for the PLL with the divider of Section 3.4 is 100MHz. In general, the PLL loop bandwidth is set below one tenth of the reference frequency, capping  $\omega_n$  at  $2\pi \cdot 10\text{MHz}$ . For this thesis, an even lower value is used, which allows for a larger divide ratio between the output and reference frequencies, as well as ensuring that the pole of the control voltage buffer described below is sufficiently

high in frequency that it will not affect loop dynamics. Therefore,  $\omega_n$  is chosen to be  $2\pi \cdot 1.5\text{MHz}$ . The lowest reference frequency is achieved when the divide ratio  $N = 16$ , which, from Equation 3.7, leads to a  $C_{PLL}$  of 16pF.

For optimum settling times and no peaking in the frequency response, the damping factor  $\zeta$  should be 0.707. This corresponds to  $R_{PLL} = 6.6k\Omega$ . Upon simulating the circuit, however, this proved to be inadequate for reasonable settling characteristics. The PLL has additional poles from  $C_{HOP}$  in the loop filter and the voltage control buffer, as well as the delay term from the divider, so the second order approximation is only useful for initial hand calculations. From simulations, a final  $R_{PLL}$  value of  $7.5k\Omega$  was chosen. This places the open loop zero at a slightly lower frequency than the unity gain crossover frequency, which increases the phase margin.

All of the above calculations assumed a divide value of sixteen. The divider is also capable of dividing by eight. Equation 3.7 states that halving  $N$  causes  $\omega_n$  and the damping factor  $\zeta$  to each increase by  $\sqrt{2}$ . The higher damping factor means that the resultant stability of the loop is helped by the lower divide value, and no consideration is made to increase the loop bandwidth along with the higher reference frequency.

### 3.4 Divider

The divider design is kept deliberately simple in this design, since the focus of the design work is on the VCO. The divider simply divides by eight or sixteen. This allows for an off-chip reference frequency of less than 200MHz. For an actual implementation, this is a very high reference frequency since the fastest crystal oscillators only operate up to 133MHz. In addition, the lack of intermediate divide values limits the frequency resolution of the output, but a different divider could easily be added to overcome these obstacles. A simplified divider schematic is shown in Figure 3-8, and a complete schematic is shown in Figure A-4.

The divide by eight circuit is simply four registers,  $X_1$ – $X_4$ , whose output is cross-coupled to its input. This is a synchronous divider configuration and requires all of the registers to work at the maximum frequency but has better jitter performance

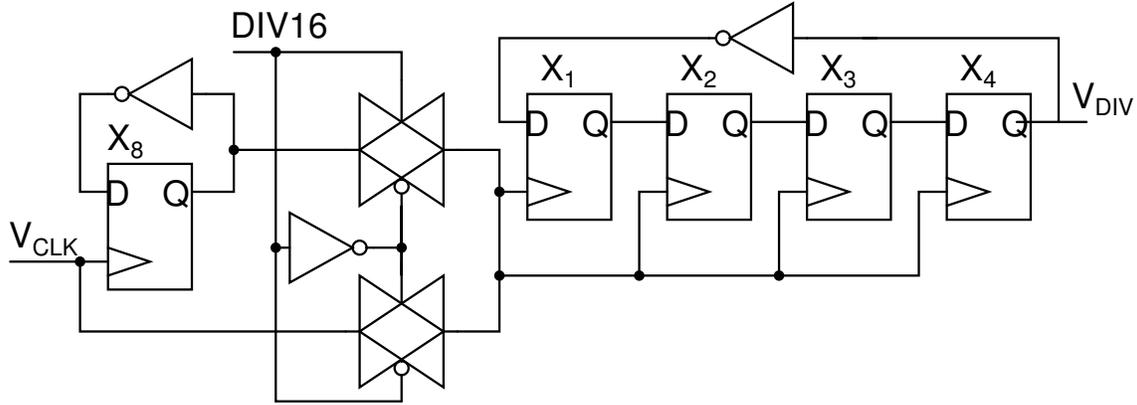


Figure 3-8: Simplified divider schematic. All signals except  $DIV16$  are differential

since the jitter in  $X_1-X_3$  does not impact the jitter of the output. The inverter in the feedback path is implemented by switching the two wires that carry the differential output  $V_{CLK}$ .  $X_8$  performs a divide by two operation, and either its output or the high speed  $V_{CLK}$  is used to clock the divide by eight subcircuit, as selected by  $DIV16$ .

All of the registers are positive edge triggered and implemented using two CML latches. Since the output of the VCO is sinusoidal, it is passed through a limiting amplifier to produce a square wave before being passed to the divider.

While this divider functions in simulation, it cannot be guaranteed to operate correctly as is. The problem is that for the divide by eight circuitry to function properly, all of the registers must start up with the same output voltage; however, if, for instance, the outputs of  $X_1-X_4$  start up as 1,0,1,0, respectively, then the divider produces three rising edges on its output for every eight input clock cycles. Another implementation of the synchronous divide by eight circuit that does not have this limitation is shown in Figure 3-9 [51].

### 3.5 Control Voltage Buffer

The total amount of capacitance that is connected to the control voltage in the VCO is slightly less than 29pF, when all of the banks are activated. As this amount is more than the total capacitance in the loop filter,  $V_{CTL}$ , the output of the loop filter, must

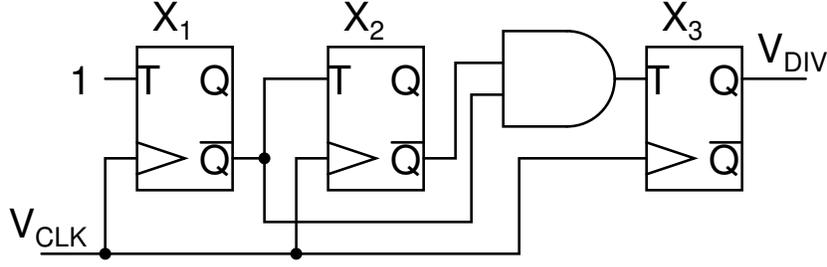


Figure 3-9: Synchronous divide by 8 circuit implementation that does not depend on startup conditions for proper operation [51].  $X_1$ – $X_3$  are toggle registers.

be buffered before the VCO. Since the PLL dynamics will be affected by any added poles, the buffer needs to be sufficiently fast that its pole is well above the bandwidth of the PLL. The buffer has rail-to-rail input and output so that each bank in the VCO can have maximum tuning range. The final schematic of the control voltage buffer is presented in Figure 3-10.

The circuit is a rail-to-rail input and output operational transconductance amplifier in a unity gain feedback configuration. The loop filter output is connected to  $M_{N1}$  and  $M_{P1}$ , which is the non-inverting input. The output  $V_O$  is fed back to  $M_{N2}$  and  $M_{P2}$ , the inverting input. As  $V_{CTL}$  goes towards the positive rail,  $M_{P1}$  turns off, but  $M_{N1}$  remains on, and  $M_{P9}$  pulls up  $V_O$ . As  $V_{CTL}$  drops towards  $V_{SS}$ ,  $M_{N9}$  pulls down the output. The simulated DC transfer curve of this circuit is shown in Figure 3-11. As can be seen, the performance is highly linear between 0.1 and 1.1V, allowing for a wide  $V_{CTL}$  swing.

The dominant pole of the buffer is at its output and is located at  $p_1 = 1/((r_{op9} \parallel r_{on9})C_L)$ , where  $C_L$  includes the parasitic capacitance of  $M_{P9}$  and  $M_{N9}$  as well as the load capacitance presented by the varactors of the VCO. The output resistance is determined from simulations as  $R_o = 6.4k\Omega$ . Without any load capacitance, the non-dominant poles cause the circuit to be close to unstable at high frequencies. The open loop (i.e. no connection between  $V_O$  and the inverting input) transfer function is plotted in Figure 3-12. While the circuit does have a crossover frequency at 7.37GHz, its phase margin is only 12.5°. As can be seen in the closed loop response of Figure 3-13, with no capacitive load on the output, this low phase margin translates into



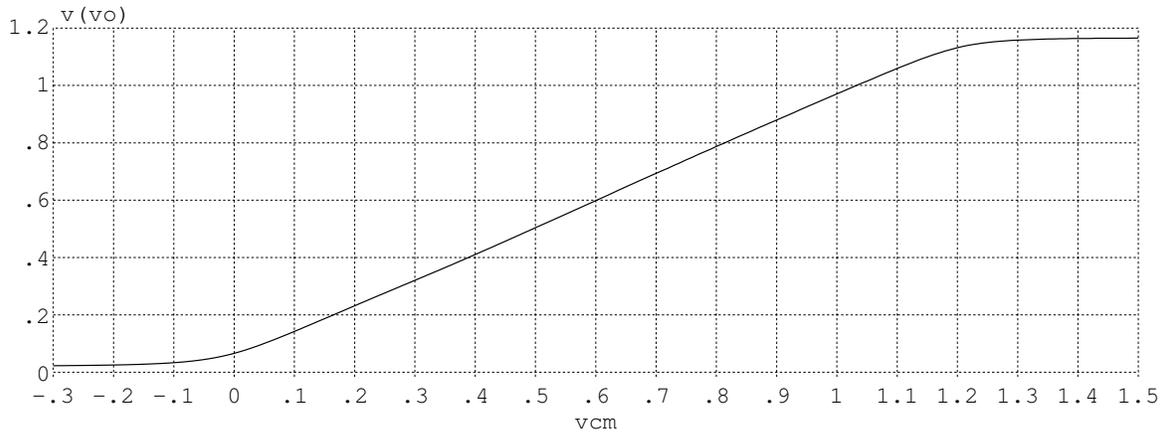


Figure 3-11: DC transfer curve of the control voltage buffer

safe to ignore in the loop filter calculations.

### 3.6 Summary

The overall phase-locked loop design, while not the principal focus of this thesis, is useful since it provides a mechanism to compensate for nonlinear behavior in the VCO as well as complement the tuning range of the VCO. A tristate phase-frequency detector is used to determine the phase error between the reference and divided output clock. This topology eliminates problems that can arise from simpler phase detectors that can lock onto higher harmonics of a clock, which is especially important because the VCO frequency can vary by a factor of two.

The loop filter includes an integrator so that the loop can lock away from the center frequency of the VCO. In addition, to maximize the tuning range of any single VCO capacitor bank, the control voltage can vary from almost rail-to-rail. This increases the amount of overlap between banks. A unity gain buffer is placed between the loop filter and the VCO. This buffer is capable of driving the large amount of capacitance connected to  $V_{CTL}$  and can operate with both its input and output going nearly rail-to-rail.

The VCO is nonlinear since its gain changes as more banks are activated. The modified charge pump compensates for the  $K_{VCO}$  variation. The  $K_{VCO}I_{CP}$  product

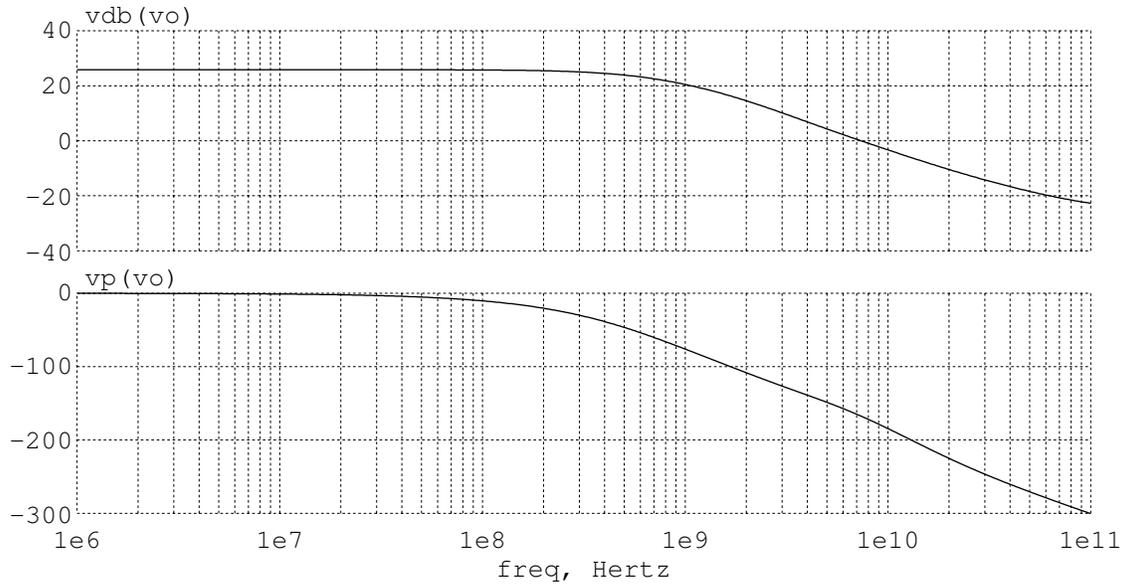


Figure 3-12: Simulated open loop transfer function of control voltage buffer without load capacitance

still varies slightly over the entire tuning range because  $I_{CP}$  only takes on four discrete values; however, this variance can be lowered by increasing the number of transistors, and properly ratioing them, in the implementation of the charge pump current source.

The frequency divider is very simple and does not allow for high resolution on the output of the VCO. A more complicated divider, however, could easily be included to provide higher resolution if that is desired.

The design and analysis of the individual building blocks of the phase-locked loop has been presented in this chapter. Simulation results of this design can be seen in the next chapter.

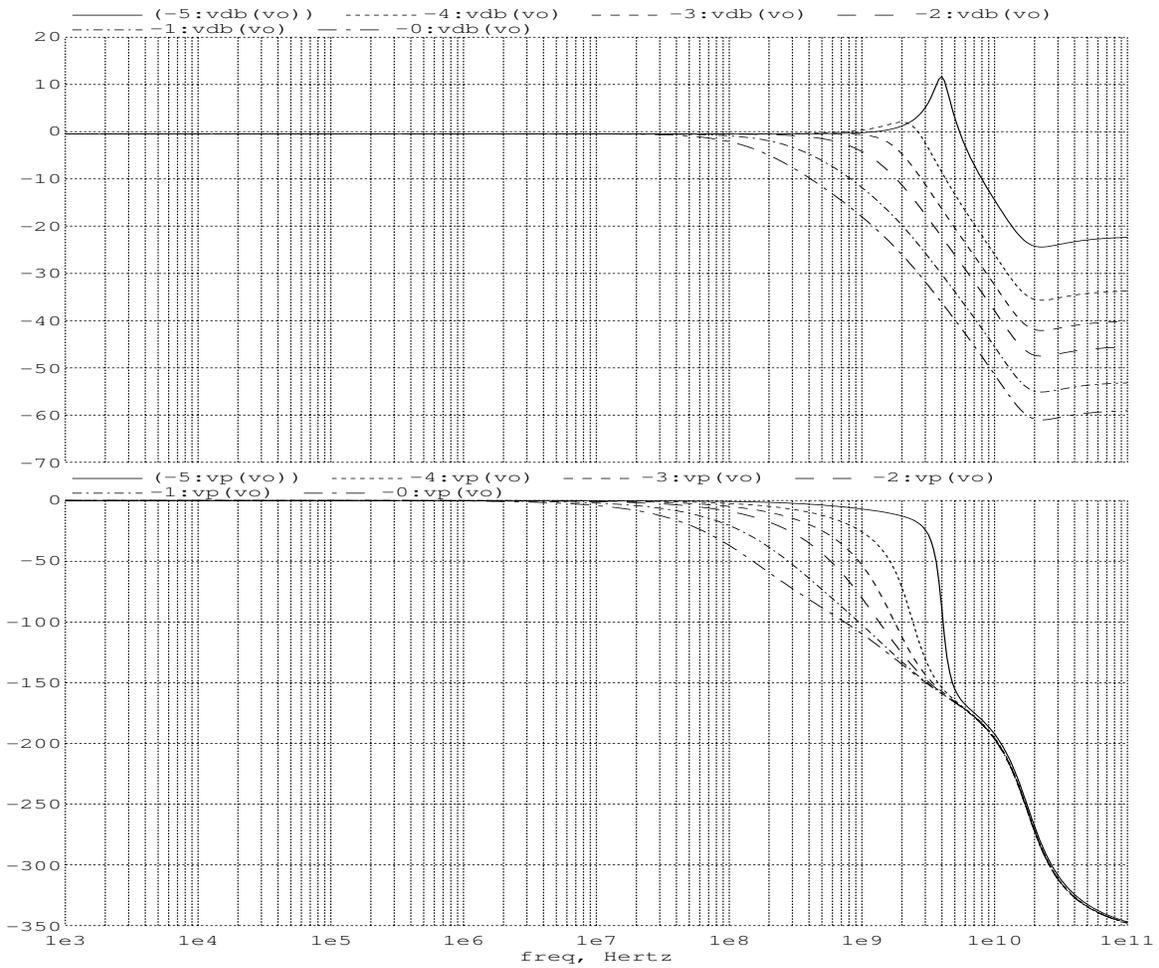


Figure 3-13: Simulated closed loop transfer function of control voltage buffer for values of the load capacitance of 0pF, 200fF, 500fF, 1pF, 2.5pF, and 5pF

# Chapter 4

## Simulation Results

This chapter presents the simulation results for both the VCO as a standalone circuit and the entire PLL. All simulations were done using Adice, Analog Devices' proprietary simulation software. The first section gives some of the details related to the simulation not mentioned elsewhere, including inductor design and wiring capacitance considerations.

The VCO simulations of Section 5.2 fall into three categories. The first includes transient simulations showing the startup and step response of the VCO, which is used to confirm that the amplitude and control loops are stable as well as showing the results of the quadrature mode forcing circuitry. Next are results from a sweep of the control voltage and the different capacitor banks to measure the overall frequency range, power consumption at different frequencies, and phase accuracy at these frequencies. Finally, a detailed phase noise analysis is presented.

Section 5.3 presents the results of the PLL simulations. While this section only shows transients from two different reference frequencies, the PLL was tested over the full frequency range because the dynamics of the different components in the PLL vary significantly over this range, particularly  $K_{VCO}$  and  $I_{CP}$ . The last section summarizes the simulation results and compares them to the design targets.

## 4.1 Simulation Overview

All of the simulations for this thesis use a TSMC  $0.13\mu\text{m}$ ,  $1.2\text{V}$  CMOS process with RF option. The process has eight metal layers and one polysilicon layer. The RF option contains an extra thick ( $3\mu\text{m}$ ) top metal layer suitable for making high Q inductors. A T-coil inductor layout, as shown in Figure 4-1, is simulated using the model of Figure 4-2. One T-coil is used for each of the cores. The voltage at  $L_{1TAP}$  is the small signal inverse of the voltage at  $L_{2TAP}$ , so the mutual inductance of the inductors serves to increase each one's effective inductance without adding extra series resistance or parasitic capacitance, thereby increasing the Q of the inductor. The actual self and mutual inductance values were computed by FastHenry [52], a free inductance modelling software package available from MIT. The final values used in the model are a self inductance of  $0.70\text{nH}$ , a mutual inductance coupling coefficient of  $0.63$ , and a series resistance of  $1.28\Omega$ . Thus the effective inductance value is  $1.14\text{nH}$ , and the Q of the inductor circuit is  $13.4$  at  $2.4\text{GHz}$ , the center frequency of operation. In general, a higher Q tank requires less power and will result in a VCO with lower phase noise, and with this Q, the series resistance of the inductor is not a significant contributor to the phase noise, as shown in Section 4.2.6.

This thesis does not include any layout, with the exception of the general layout for the inductor. Very few nodes would actually have enough wiring capacitance to affect their performance, especially considering that all blocks except for the VCO and divider are operating at a maximum speed of  $400\text{MHz}$ . The VCO, however, not only is sensitive to the amount of wiring capacitance on its tank nodes, but the number of connections to these nodes, including 22 capacitor banks per node, would mean a large amount of wiring capacitance. To model this capacitance as well as any loading capacitance from buffers used to distribute the clock throughout the chip, a  $500\text{fF}$  fixed capacitance is included on each of the four output nodes of the VCO. This is a rather conservative estimate based on similar designs in a  $0.18\mu\text{m}$  process, but once a layout is done and the actual load capacitance is known, an integrated capacitor can be inserted to make up any difference without affecting the VCO performance.

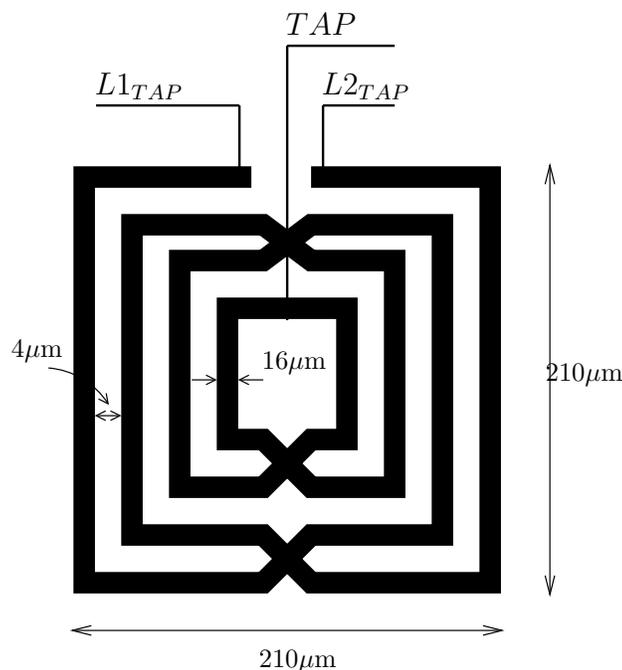


Figure 4-1: Layout of the T-coil inductor. It functions as two inductors if the  $L1_{TAP}$  and  $L2_{TAP}$  terminals are inverses of each other.

Of course, if the load capacitance turns out to be much smaller, the VCO will be able to achieve a higher frequency, and more capacitor banks could be added to increase the tuning range further.

## 4.2 VCO Simulation Results

### 4.2.1 Startup Transients

When the VCO is not oscillating, the amplitude control loop forces the VCO to have a very high gain, which causes any perturbation to grow exponentially until the target amplitude is met. In a fabricated circuit, thermal noise is sufficient to cause this initial perturbation. In simulations, a small impulse of charge is injected at time 0 to mimic this random noise. The figures in this section correspond to the startup of the VCO at the highest frequency bank and a steady-state frequency of 3.215GHz. In this particular simulation run, the VCO starts up in the wrong quadrature mode, and the effect of flipping quadrature modes can be seen.

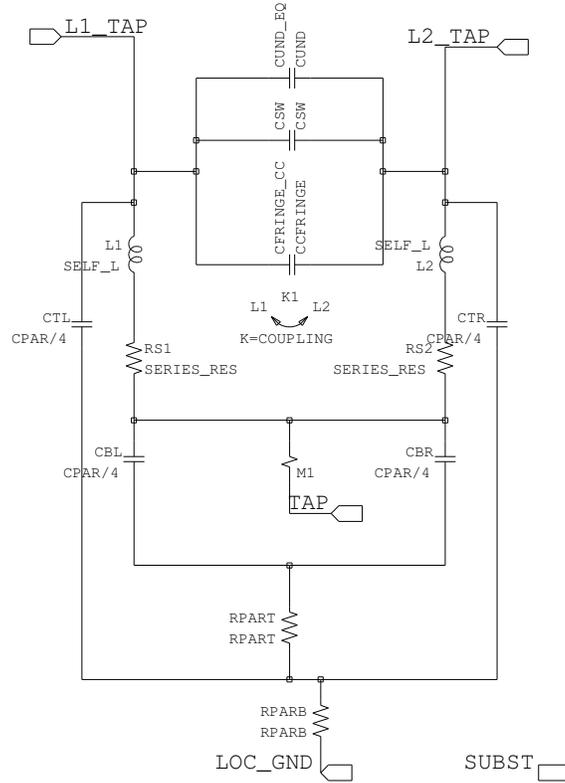


Figure 4-2: Simulation model of the T-coil inductor

Figure 4-3 shows the differential outputs after startup. Initially, the amplitude control loop forces a lot of current through the VCO until it has started up. The output amplitude grows and only starts to fall as the amplitude control loop settles. The spikes around 85ns are the result of the VCO switching its quadrature mode. Figure 4-4 is an enlarged picture of this region. At the start of the transition,  $V_{OQ}$  is  $90^\circ$  after  $V_{OI}$ , and at the end of the transition, this has reversed.

The settling of the common mode loop can be seen in Figure 4-5. The figure shows the voltage at  $TI$ , the node connecting the two inductors in the first core. Before the quadrature phase transition, the signal has a relatively high peak-to-peak amplitude, which occurs because the current in the core is very high at this point, which increases the nonlinearities of the devices, and the resultant even order harmonics show up on  $TI$ .

When the quadrature phase correction circuit turns off, it creates a step drop in current, which causes the voltage at  $TI$  to step up at 90ns. The resultant step response

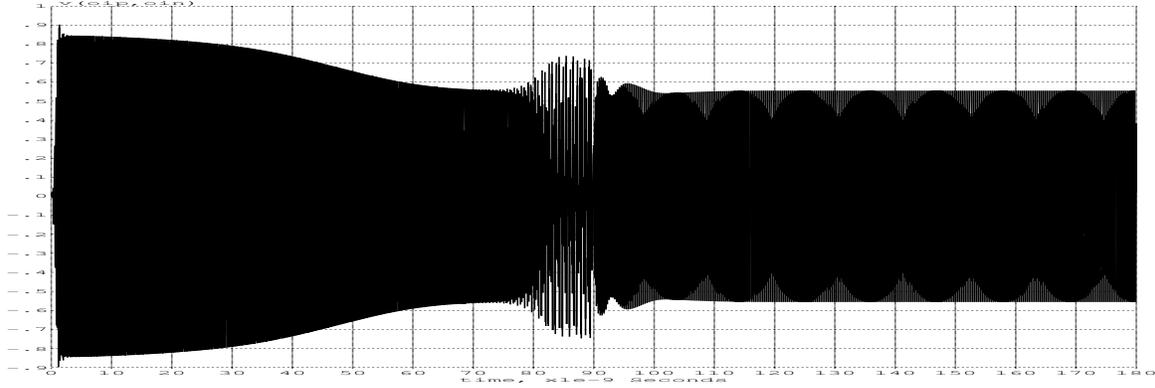


Figure 4-3: Differential output voltage  $V_{OI} = V_{OIP} - V_{OIN}$  as the VCO settles after startup

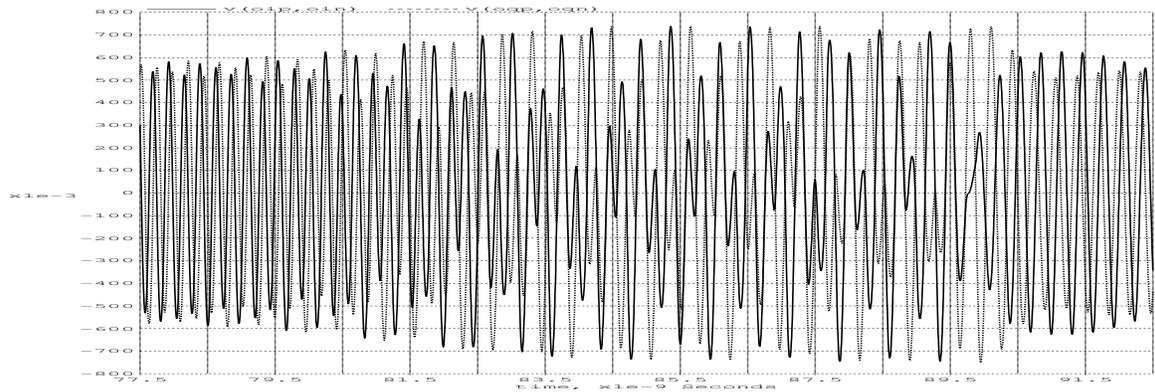


Figure 4-4: Zoom in on output voltage as the quadrature control circuit transitions from the higher frequency mode to the lower frequency, stable mode

shows a peak overshoot of 17%, slightly more than the theoretical case, which is a result of ignored parasitic poles in the OTA and the pullup resistor implementation. Since the current through the core is much less after the quadrature phase reversal, so is the ripple on  $TI$ .

Figure 4-6 shows the settling of  $V_{PEAK}$ , which is the amplitude as measured by the peak detector. Before 85ns, this plot follows the shape of the output amplitude of Figure 4-3. At 90ns, the amount of current in the tank experiences a step decrease as the quadrature mode forcing circuitry turns off. The amplitude also experiences a step drop at this point because it approximately follows the current in the tank. The resultant settling of  $v_{PEAK}$  shows the step response of the loop. This loop has

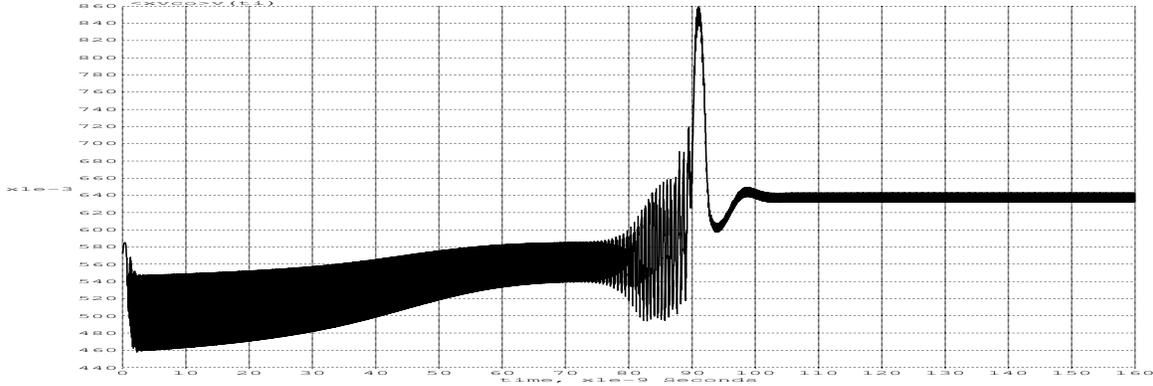


Figure 4-5: Settling of the common mode control loop as observed at  $TI$ , the common tap of the inductors in the first core. The tank experiences a step in a current and therefore a step in common mode point of the circuit at 90ns, corresponding to the quadrature mode forcing circuit turning off.

slightly worse dynamics than the common mode control loop, experiencing almost 66% peak overshoot, though there is very little ringing. A normal second order system underdamped enough to produce that much overshoot has much more ringing. This has little ringing because the overshoot is not caused by the amplitude control loop alone. The common mode point of the output (Figure 4-5) is also dropping at this point after the step at 90ns. The drop in common mode point will cause the peak detector's output to also drop, which makes the peak look larger than it is. The lack of any ringing shows that the interaction between the control loops, as explained in Section 2.5.3, does not make either one unstable.

The instantaneous frequency of the VCO output is shown in Figure 4-7. The frequency is much higher before the quadrature control loop switches modes, as predicted in Section 2.3.1.

## 4.2.2 Response to Step in Power Supply Voltage

Ideally, the VCO should oscillate at a frequency independent of  $V_{DD}$ . The amplitude and control loops set the current and common mode points of the oscillator, and the reference voltages for these loops are generated using a cascode current source driving a resistor referenced to ground. In practice, though, the finite output impedance of

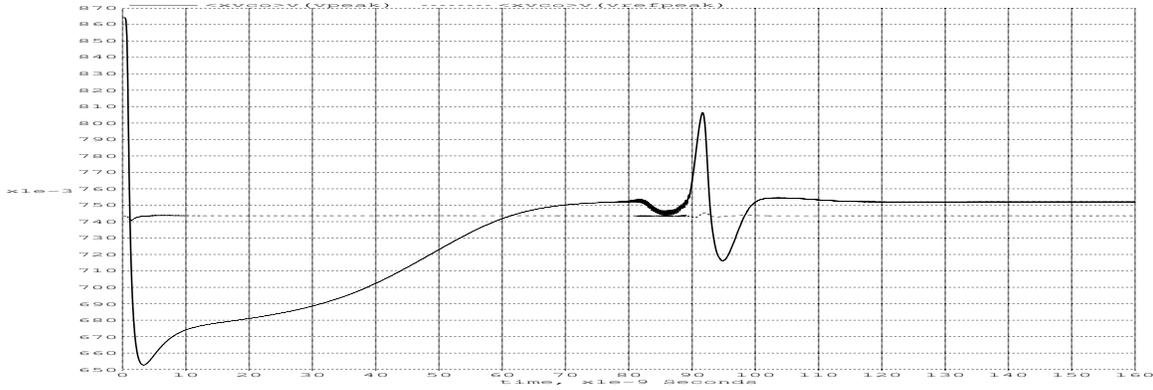


Figure 4-6: Settling of the amplitude control loop, as observed at  $V_{PEAK}$ , the output of the peak detector.

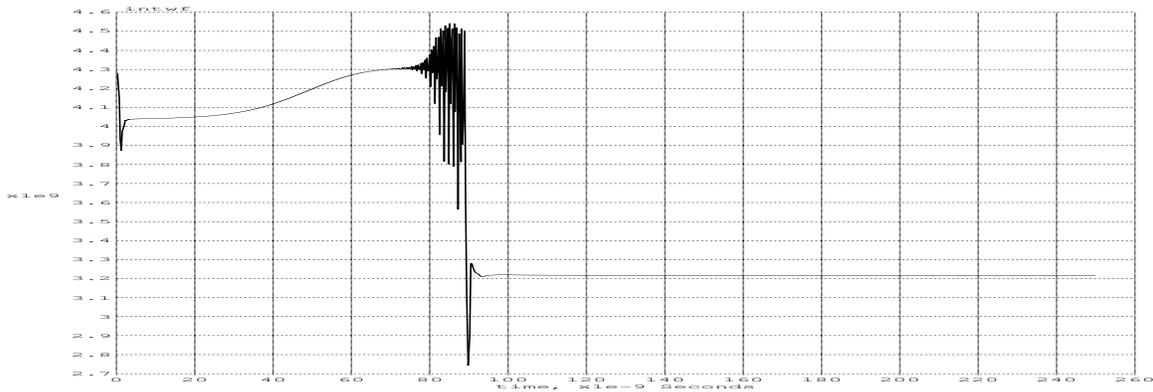


Figure 4-7: Instantaneous frequency of the VCO versus time as the VCO settles after startup. The frequency is measured only at zero crossings of  $V_{OI}$ .

the cascode current source as well as the non-zero steady state error to a step input in both of these loops cause the VCO's output frequency to change in response to a step in the power supply.

Figure 4-8 shows the response of the instantaneous frequency when  $V_{DD}$  is raised from 1.2V to 1.26V, an increase of 5%. Initially, the common mode point of the VCO increases with the step in supply, raising the bias across the varactors and thereby increasing their capacitance and lowering the oscillation frequency. The common mode control loop then lowers the bias voltage, but since there is no integrator in the loop it has a non-zero steady-state error to a step input, and the common mode point never fully returns to the original 0.65V, causing a frequency error of 7MHz or

0.22%. When the VCO is running in a closed-loop PLL, this center frequency shift is compensated for by a change in  $V_{CTL}$ .

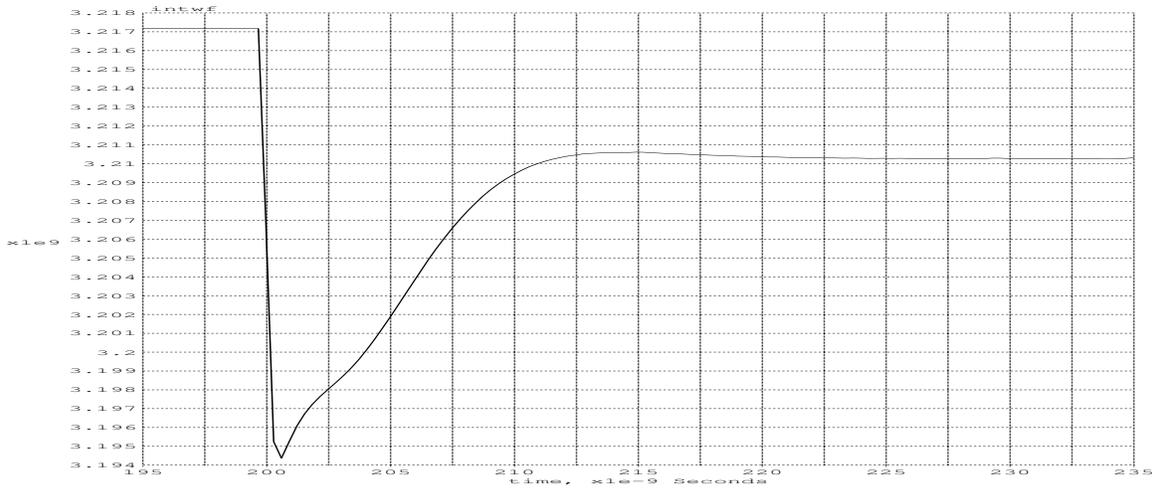


Figure 4-8: Instantaneous frequency of the VCO in response to a step of  $V_{DD}$  from 1.2 to 1.26V at 200ns

### 4.2.3 Tuning Range

The tuning characteristic of the VCO was calculated by running transient simulations for each of the banks over the entire range of  $V_{CTL}$ . Piecing the results of these simulations together, the total tuning characteristic is shown in Figure 4-9. Each curve represents one capacitor bank, with more capacitors switched in going down the graph. The actual usable range of  $V_{CTL}$  is limited to 0.1 to 1.1V, which means that the total tuning range of the VCO is 1.488 to 3.281GHz, at nominal conditions. The tuning range data for each of the banks is shown in Table 4.1.

The maximum  $K_{VCO}$  for each bank is when  $V_{CTL}$  is around 0.65V. This matches the prediction because that is when there is zero DC bias across the varactors and therefore the maximum slope on the varactor tuning curve of Figure 2-15.  $K_{VCO}$  increases, as predicted, when the VCO is in its lower frequency banks, and this leads to a much higher overlap percentage between banks at lower frequencies. The overlap between two successive banks is 55.9% at its minimum under nominal conditions.

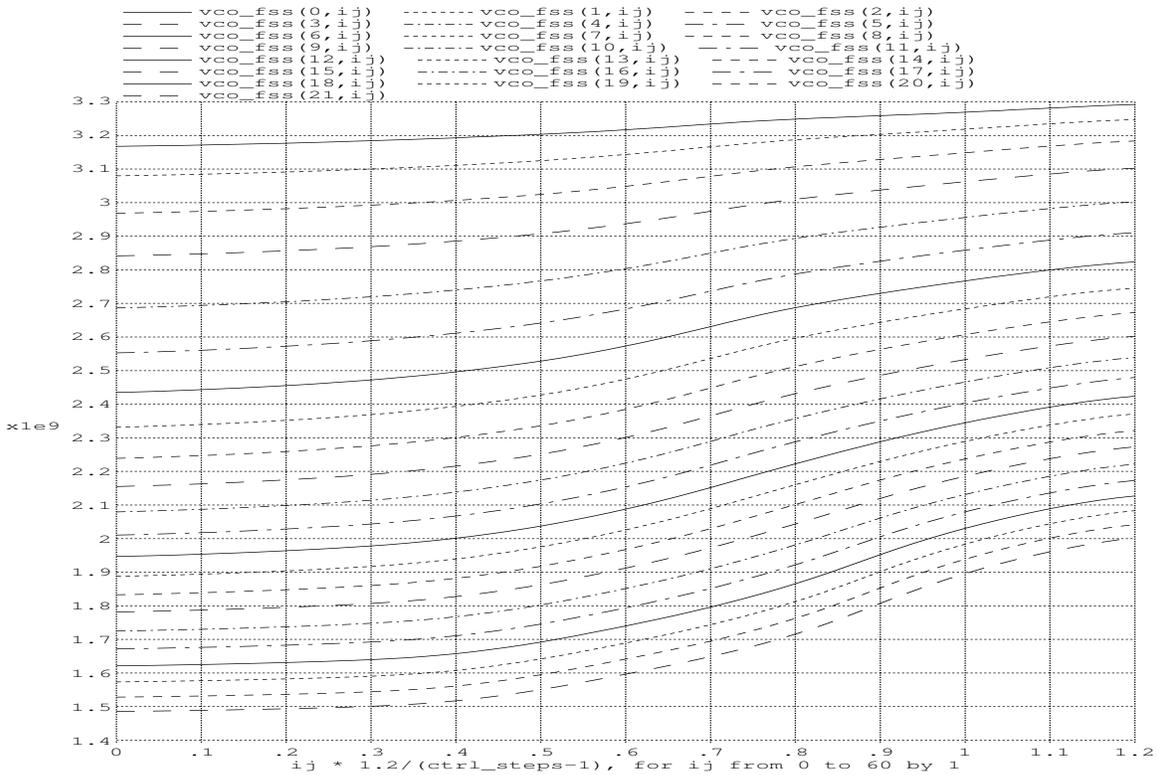


Figure 4-9: Frequency versus control voltage over all banks. Each successive curve down the plot has an extra capacitor switched in.

#### 4.2.4 Process and Temperature Variations

A real implementation of this PLL must work even under process variations and in different temperature conditions. Table 4.2 gives the performance of the circuit under four process variations (fast NFET/fast PFET, slow N/slow P, fast N/slow P, and slow N/fast P) as well as at temperatures of 0°C, 27°C, and 100°C. In terms of circuit performance, the worst corner is hot and slow. At this point, the  $g_m$  through all the transistors is decreased because  $\mu$ , the mobility of the carriers, decreases at higher temperatures. In fact, without the amplitude control loop, the VCO fails to start up at this corner.

Table 4.1: Tuning range data at 27°C with nominal process parameters. Maximum and minimum frequencies are measured with  $V_{CTL_{max}} = 1.1V$  and  $V_{CTL_{min}} = 0.1V$ , respectively.

Bank Number	Max. Frequency (GHz)	Min. Frequency (GHz)	Span (MHz)	Overlap with next bank (%)	Avg. Current (mA)
0	3.281	3.171	109.9	57.32	8.18
1	3.234	3.084	149.9	55.85	8.87
2	3.168	2.974	194.3	57.27	9.71
3	3.085	2.847	237.7	56.82	10.9
4	2.983	2.694	288.6	67.41	12.4
5	2.889	2.561	327.9	72.90	13.9
6	2.800	2.443	356.4	77.51	15.4
7	2.720	2.340	379.9	80.42	16.8
8	2.645	2.247	398.1	82.00	18.0
9	2.574	2.163	410.5	84.23	19.6
10	2.509	2.087	421.6	85.64	20.7
11	2.448	2.018	430.6	86.80	22.0
12	2.391	1.954	437.8	87.78	23.0
13	2.338	1.894	443.7	88.62	24.2
14	2.289	1.839	448.6	88.95	25.3
15	2.238	1.787	450.6	88.37	26.7
16	2.185	1.730	455.4	89.12	28.4
17	2.136	1.676	459.7	89.78	29.9
18	2.089	1.625	463.7	90.36	31.7
19	2.044	1.577	467.2	90.88	33.1
20	2.001	1.531	470.0	91.33	35.1
21	1.961	1.489	471.1	—	36.8

### 4.2.5 Quadrature Accuracy

With no mismatch between the two cores, the resultant phase accuracy is only limited by the accuracy of the simulation. To model mismatch between the two tanks, the value of the capacitors in the right tank is changed by 2%, and a transient simulation is done to measure the resultant phase error. Once the circuit has reached steady-state, there is both a phase and amplitude error between the  $I$  and  $Q$  outputs of the VCO. Figure 4-10 shows the two outputs in steady-state.

The phase difference between the  $I$  and  $Q$  outputs is plotted versus the control

Table 4.2: Performance of VCO under process and temperature variations

NFETS	NFETS	Temp. (°C)	Min. Frequency (GHz)	Max. Frequency (GHz)	Minimum overlap (%)
N	N	0	1.517	3.289	57.23
N	N	27	1.489	3.281	55.85
N	N	100	1.453	3.268	51.58
F	F	0	1.586	3.298	54.13
F	F	27	1.574	3.289	53.55
F	F	100	1.534	3.269	46.47
S	S	0	1.412	3.280	37.08
S	S	27	1.407	3.257	51.66
S	S	100	1.397	3.254	38.94
F	S	0	1.545	3.278	57.16
F	S	27	1.534	3.271	53.52
F	S	100	1.479	3.252	48.90
S	F	0	1.448	3.291	52.21
S	F	27	1.445	3.284	55.79
S	F	100	1.387	3.273	51.35

voltage for each of the 21 banks in Figure 4-11. This error is significantly larger in magnitude than that predicted in Section 2.3.3, but that section only considered first order effects. Increasing  $m$ , the coupling coefficient between the two cores, can lower this phase error but only at the expense of more power.

## 4.2.6 Phase Noise

### Simulation methodology

The phase noise is calculated using the procedure suggested by Hajimiri and Lee [30]. The VCO behaves as a linear, time-variant system in response to noise. For instance, noise injected into the circuit when the output is at a voltage maximum ideally produces no change of the output phase, whereas noise injected when the output is at zero significantly affects the zero crossings. Hajimiri uses an impulse sensitivity function (ISF) to model the phase response of the VCO over one period of oscillation. An impulse of charge is inserted at a time offset  $\tau$  from the start of

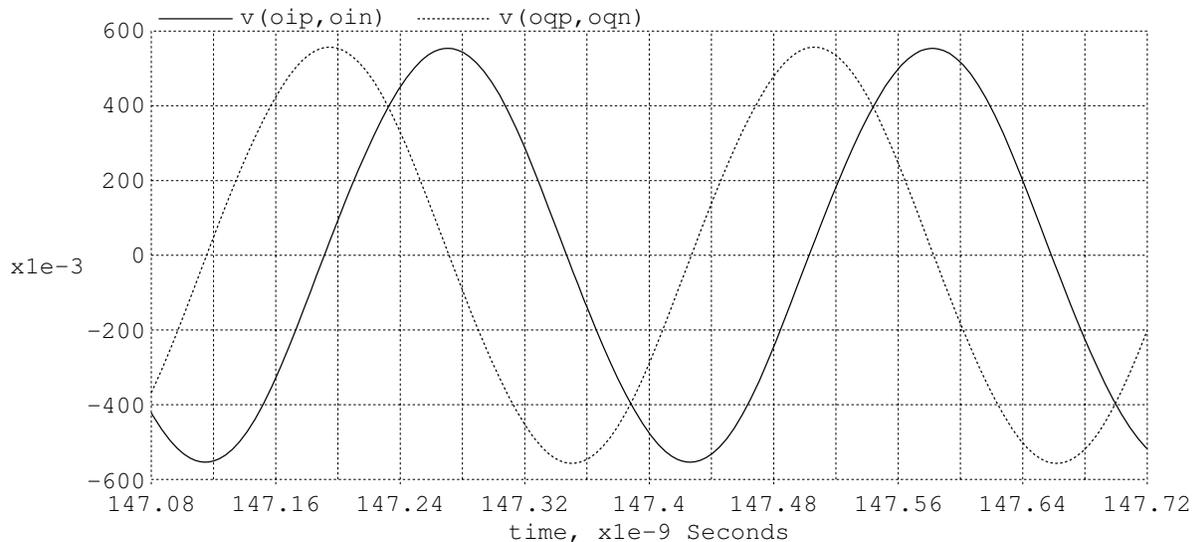


Figure 4-10: Steady-state output of the VCO with 2% capacitor mismatch between the two tanks

one oscillation period. The resultant phase error  $\Delta\phi$  is measured many cycles later, and this process is repeated as  $\tau$  varies over one period. Thus, for any specific  $\tau$ , the impulse response of the phase is a step function of height  $\Delta\phi(\tau)$ . The following function defines the impulse response of the phase for an impulse injected at  $\tau$  after the start of the oscillation period:

$$h_\phi(t, \tau) = \frac{\Gamma(\omega_0\tau)}{q_{\max}} u(t - \tau), \quad (4.1)$$

where  $q_{\max}$  is the maximum charge across the capacitor. In this equation,  $\Gamma(x)$  is the ISF, and it is defined as the resultant phase delay when a current impulse of size  $q_{\max}$  is injected at time  $x$ , where  $x$ , varying from 0 to  $2\pi$ , is the phase in radians of the output oscillation when the impulse occurs.

The ISF is specific to the node where the charge is injected. In addition, the definition of the ISF assumes that the circuit responds to noise in a linear fashion. Injecting a charge of  $q_{\max}$ , however, is large enough that the linear approximation fails, so only a small amount of charge  $q_\epsilon$  is added. Define  $\Psi(\tau)$  as the resultant phase difference, divided by  $q_\epsilon$ , when charge is inserted at time  $\tau$  into a node. Then  $\Gamma(x) = \Psi(\tau)q_{\max}|_{\tau=x/\omega_0}$ . Hajimiri calculates the phase noise contribution of a current

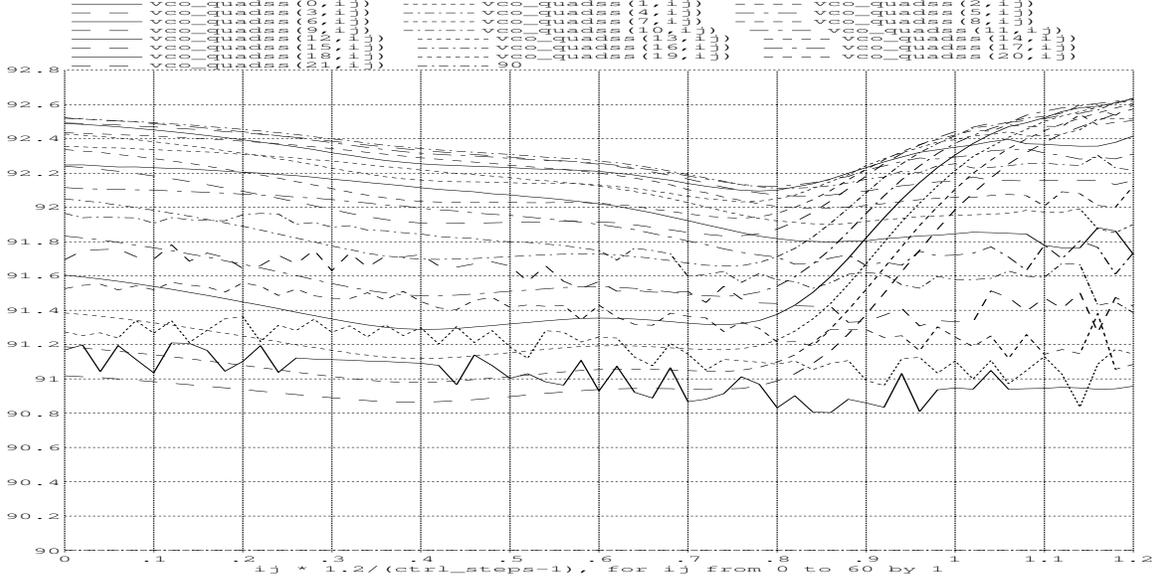


Figure 4-11: Steady-state phase difference between  $I$  and  $Q$  outputs when the capacitors in the  $Q$  tank are 2% larger than those in the  $I$  tank

noise source, in the  $1/f^2$  region, as

$$\mathcal{L}\{\Delta\omega\} = 10 \log \left( \frac{\Gamma_{\text{rms}}^2}{q_{\text{max}}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{4\Delta\omega^2} \right). \quad (4.2)$$

Since  $q_{\text{max}}$  is difficult to measure, it is more direct to work with  $\Psi(\tau)$ , which can be calculated directly from the measured phase error by dividing by a known  $q_\epsilon$ . Noting that

$$\Gamma_{\text{rms}}^2 = \frac{1}{2\pi} \int_0^{2\pi} |\Gamma(x)|^2 dx = \frac{1}{2\pi} \int_0^{2\pi} |\Psi(\tau)|^2 q_{\text{max}}^2 \omega_0 d\tau = \Psi_{\text{rms}}^2 q_{\text{max}}^2, \quad (4.3)$$

Equation 4.2 is equivalent to

$$\mathcal{L}\{\Delta\omega\} = 10 \log \left( \frac{\Psi_{\text{rms}}^2 q_{\text{max}}^2}{q_{\text{max}}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{4\Delta\omega^2} \right) = 10 \log \left( \Psi_{\text{rms}}^2 \frac{\overline{i_n^2}/\Delta f}{4\Delta\omega^2} \right). \quad (4.4)$$

Therefore, the phase noise can be calculated without needing to know the specific value of  $q_{\text{max}}$ .

For every noise source, an ISF must be determined, since injecting charge into different nodes affects the output phase differently. All transistor noise is modelled as a current source connected between its drain and source terminals, with the actual

magnitude of this noise source determined from simulation. Resistors have thermal noise, which is modelled as a current source in parallel with the the resistor with variance  $\overline{i_{nR}^2} = 4kT\Delta f/R$ . The capacitors are modelled as a subcircuit including the capacitor, parasitic resistance, and in the case of the N-well varactors, a diode to substrate. The noise contributions of the parasitic resistance and diode are also included in the total noise contribution.

## ISF results and interpretation

Figure 4-12 is  $\Gamma(x)/q_{\max}$  when charge is injected directly into one of the output nodes of the VCO and  $x$ , the independent variable, is the phase of that same node's signal. As would be expected, the ISF is periodic with period  $2\pi$ . At the zero crossings of the output ( $0$ ,  $\pi$ , and  $2\pi$  radians), the magnitude of the ISF is at a near maximum, and the ISF is at a minimum at roughly  $\pi/2$  and  $3\pi/2$  radians, when the output is at a voltage maximum. The ISFs for charge injected at the other three output nodes have exactly the same shape but are phase shifted by  $\pi/2$ ,  $\pi$ , or  $3\pi/2$ , which matches intuition since the quadrature loop forces each of these outputs to be  $\pi/2$  away from each other. These ISFs, as well as all the other ones used in the phase noise calculation are included in Appendix B. If a node has a voltage signal that is at twice the frequency, such as at *ICOM* in Figure 2-2, the corresponding ISF is also at twice the fundamental frequency.

Table 4.3 lists the top ten contributors to the phase noise at 3.216GHz. Both the variance of the noise source and  $\Psi_{\text{rms}}$  are listed. The largest contributor  $R_5$  sets the reference voltage  $V_{REFPEAK}$  for the amplitude control loop, as shown in Figure 4-13. The phase noise contribution of this resistor, though, can be improved by drawing more power. If the thermal noise of the resistor is modelled using a current source in series with  $R_5$  with  $\overline{i_{nR_5}^2} = 4kT\Delta f/R_5$ , then the ISF for that thermal noise source is linearly dependent on the value of  $R_5$ , since the following stage only responds to the actual voltage at  $V_{REFPEAK}$ . Since  $\Gamma \propto R_5$  and  $\overline{i_{nR_5}^2} \propto 1/R_5$ , then from Equation 4.2,  $\mathcal{L}(\Delta\omega)$  will increase at a rate of 10dB/decade with  $R_5$ . A smaller  $R_5$  would require more current through that leg to generate the same  $V_{REFPEAK}$ , but it would result

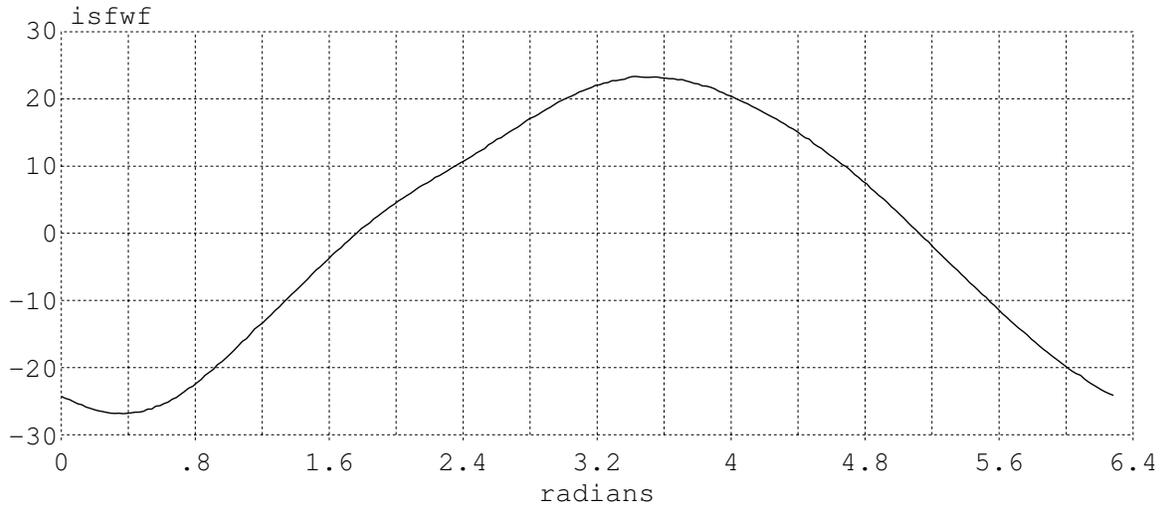


Figure 4-12: The impulse sensitivity function, scaled by  $1/q_{\max}$ , when charge is injected onto  $V_{OIP}$ , one of the output nodes of the VCO

in a lowering of  $R_5$ 's contribution to the overall phase noise.

The next six primary contributors to the phase noise are all transistors specific to the quadrature control loop. Even though these transistors have less current than the cross-coupled core transistors, they contribute more phase noise, since their impulse sensitivity function has a higher rms value. To understand this, consider the output-referred noise current of  $M_{N_5}$ , one of the quadrature coupling devices. This current is injected directly into the output node, which does not affect the phase any more than current from  $M_{N_1}$ , one of the regenerative devices; however, it is also injected into  $QCOM$ , whereas  $M_{N_1}$ 's current is injected into  $ICOM$ . At higher frequencies,  $QCOM$  is the higher impedance node because it has less parasitic capacitance than  $ICOM$ . Thus, with the same amount of current injected,  $QCOM$ 's voltage varies more, affecting the current through the quadrature loop, the output common mode voltage, and hence the instantaneous frequency of the output, which leads to an increased phase delay. The actual difference between the ISF of charge injected into  $ICOM$  and  $QCOM$  can be seen in Figures B-5 and B-6, respectively.

At lower frequencies, the primary contributors to phase noise change considerably. Table 4.4 lists the top 15 contributors to the phase noise with the VCO in the lowest frequency bank and the output frequency at 1.6 GHz. The phase noise is considerably

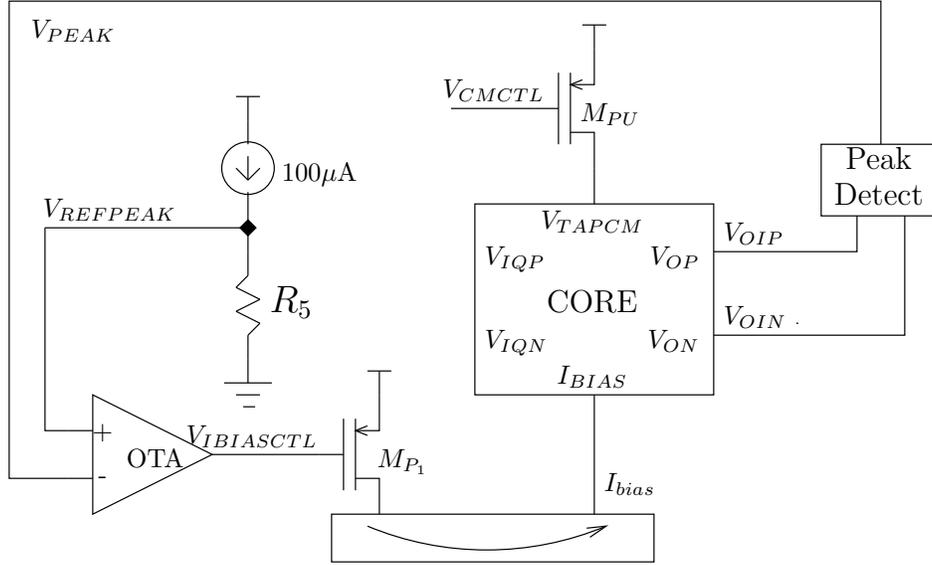


Figure 4-13: Simplified schematic of VCO showing the function of  $R_5$  in the amplitude control loop. Only one of the two VCO cores is shown.

higher at the lower frequencies. Part of this stems from the two noise sources labelled “Total switch NFETs” and “Total switch PFETs” in the table. These together represent the lumped noise contribution of all of the transmission gates for all of the switches. The total noise variance from all of these gates is very high compared to the variance of any of the other noise sources. The other cause of the increased phase noise is the increased sensitivity of the common mode and amplitude control loops at lower frequencies, as evidenced by the high ISF rms values for all of the resistors. The same argument to reduce the phase noise impact of  $R_5$  in the high-frequency case also applies to reducing the phase noise contributions of all of these resistors. By increasing the current draw through the first nine resistors listed in Table 4.4 by a factor of 10, and therefore decreasing the resistance by ten, the total phase noise drops to -103.4dBc/Hz for an increase of current of 5.5mA, or 14.8%. Still, the extra loss in the tank from the switch impedances and the increased total current required to overcome these losses prevents the phase noise from being as good at low frequencies, a fundamental limitation of this design.

Table 4.3: Top ten contributors to phase noise at 3.216GHz including the variance of the noise sources, and the rms value of their ISFs

Source	$\overline{i_n^2}$ (pA/ $\sqrt{Hz}$ )	$\Gamma_{\text{rms}}/q_{\text{max}}$	$\mathcal{L}(\Delta\omega)$ (dBc/Hz) (600MHz offset)
$R_5$	2.88	179	-117.2
$M_{N_6}$	11.30	34.5	-119.6
$M_{N_5}$	11.30	34.4	-119.6
$M_{N_{13}}$	11.61	29.8	-120.7
$M_{N_{14}}$	11.61	29.8	-120.7
$M_{N_8}$	8.20	34.5	-122.4
$M_{N_7}$	8.20	34.4	-122.4
$R_6$	1.29	211.5	-122.7
$M_{P_1}$	4.12	51.3	-124.9
$M_{N_3}$	7.96	21.4	-126.8
Total			-109.5

## 4.3 PLL Simulation Results

### 4.3.1 Startup Transients and Settling

The settling of the PLL depends on whether the VCO starts up in the correct quadrature mode; however, since the VCO is forced into the correct quadrature mode within 100ns, startup in the incorrect mode only delays the settling of the PLL. Figure 4-14 shows the settling of the control voltage  $V_{CTL}$  and the buffered control voltage  $V_{BCTL}$  as the VCO starts up in the top frequency bank, with a divide value of 8 and a reference frequency of 400MHz. In this simulation, the VCO starts in the incorrect quadrature mode, which causes it initially to have an extremely high output frequency. The PLL responds by forcing down the control voltage. Once the VCO switches into the correct quadrature mode at 75ns, the PLL then responds by settling to the correct frequency. The control voltage does not exhibit much ringing, as expected.

In the first 60ns,  $V_{CTL}$  does not fall smoothly. Instead it looks jagged from the graph. This is the cycle slipping of the tristate phase-frequency detector. In this case, the magnitude of the difference between  $\Phi_{div}$  and  $\Phi_{ref}$  becomes more than  $2\pi$ . Figure

Table 4.4: Top fifteen contributors to phase noise at 1.60GHz including the variance of the noise sources, and the rms value of their ISFs

Source	$\overline{i_n^2}$ ( $pA/\sqrt{Hz}$ )	$\Gamma_{\text{rms}}/q_{\text{max}}$	$\mathcal{L}(\Delta\omega)$ ( $dBc/Hz$ ) (600MHz offset)
$R_5$	2.88	1280	-106.2
$R_9$	1.13	2804	-107.5
Total switch NFETs	1229.2	4.6	-108.5
Total switch PFETs	938	4.6	-110.5
$R_4$	1.92	1046	-111.5
$R_2$	1.92	1046	-111.5
$R_1$	1.92	1046	-111.5
$R_3$	1.92	1046	-111.5
$R_6$	1.29	1459	-112.0
$R_8$	1.29	900	-116.2
$R_7$	1.29	900	-116.2
$M_{N_8}$	39.01	24.5	-117.9
$M_{N_{13}}$	39.01	24.5	-117.9
$M_{N_3}$	39.01	24.5	-117.9
$M_{N_4}$	39.01	24.5	-117.9
Total			-99.4

4-15 shows the input and outputs of the PFD as this cycle slipping occurs. Since the divided clock is at a much higher frequency than the reference clock, *DOWN* has a higher average value than *UP*. At 37ns, however, the phase difference has just exceeded  $2\pi$ , and in fact the reference and divided clock signal transitions line up almost perfectly, so the PFD does not tell the charge pump to further lower the control voltage. Some cycle slipping even causes *UP* to assert high longer than *DOWN*, such as at 44.2ns, which causes  $V_{CTL}$  to increase and results in its jagged appearance.

Figure 4-16 shows the PLL settling in the lowest frequency bank with a divide value of 16 and a reference clock frequency of 100MHz. The VCO actually starts up in the correct mode of quadrature, which allows the PLL to settle more smoothly, without even any cycle slipping. The plot clearly shows the long tailed transient that results from the pole-zero doublet, one of the disadvantages of a Type II PLL.

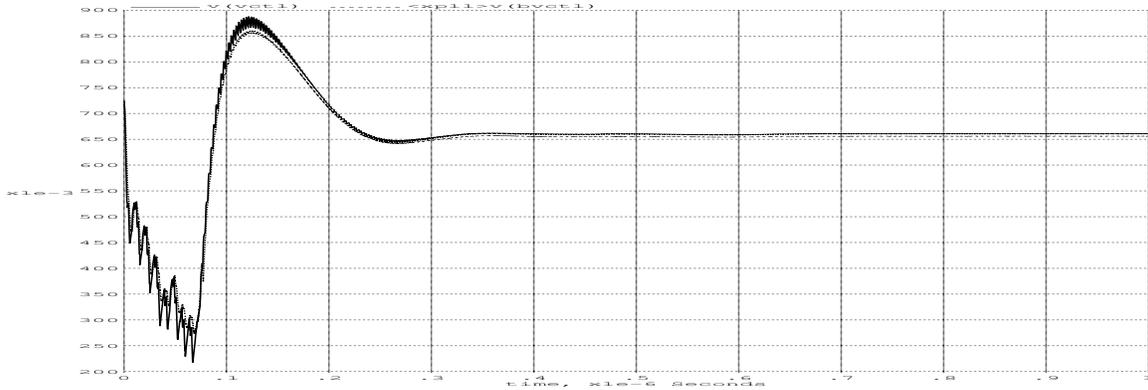


Figure 4-14:  $V_{CTL}$  startup transients as the PLL start up with 400MHz reference frequency, divide by 8, and the VCO starts up in the incorrect quadrature mode

### 4.3.2 Response to Step in Power Supply Voltage

Section 4.2.2 showed that the VCO output frequency changes in response to a step in  $V_{DD}$ , so the PLL must compensate for such a change by adjusting  $V_{CTL}$ . Figure 4-17 shows the response of  $V_{CTL}$  and the buffered  $V_{BVCTL}$  after a step in  $V_{DD}$ . The control voltage is driven to a higher voltage in steady state, since the VCO's center frequency is lower. Once again, a long-tailed transient can be seen on the settling of  $V_{CTL}$ .

### 4.3.3 Steady State Operation

Figure 4-18 shows the steady-state operation of the PLL. There is a static phase error of  $9^\circ$  between the reference clock and the divided down clock. This phase error is nonzero because the charge pump is not perfectly symmetric. The NFET on the charge pump output sinks more current than the PFET can source, so when  $UP$  and  $DOWN$  are both high before being reset, charge is removed from the loop filter, so  $UP$  must become high slightly earlier to compensate. In addition, this problem is aggravated when  $V_{CTL}$  rises because the finite output impedance of the FETs causes the PFET to source even less current. If zero steady state phase error is desired, a charge pump with higher output impedance and greater symmetry between the  $UP$  and  $DOWN$  paths must be used.

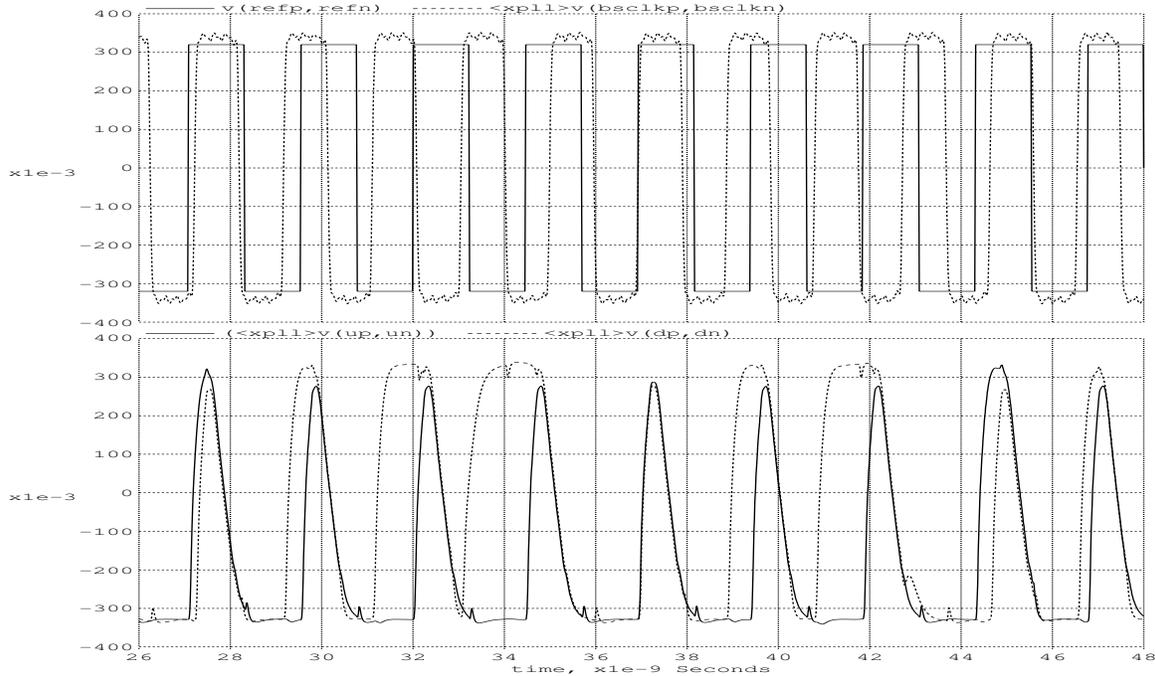


Figure 4-15: Input and output of the phase-frequency detector, showing cycle slipping as  $V_{div} = V_{bsclk}$  is at a much higher frequency than  $V_{ref}$ .

## 4.4 Summary

Table 4.5 gives a summary of the simulation results. This thesis successfully meets the tuning range and quadrature accuracy requirements targets listed in Table 1.2, even under process and temperature variations.

Table 4.5: Summary of simulation results

Tuning range (nominal conditions)	1.489-3.281 GHz
Tuning range (with variations)	1.585-3.254 GHz
Quadrature phase error (2% mismatch)	< 2.6°
Power (VCO)	8.2-38.0mA
Power (Total)	12.8-42.6mA
Phase noise at 3.217GHz	-109.47dBc/Hz at 600kHz offset
Phase noise at 1.60GHz	-99.43dBc/Hz at 600kHz offset

The largest problem with this design is the poor phase noise performance at lower frequencies as a result of the added loss in the tank from the on impedances of the capacitor bank switches. These switches not only have their own noise sources, but

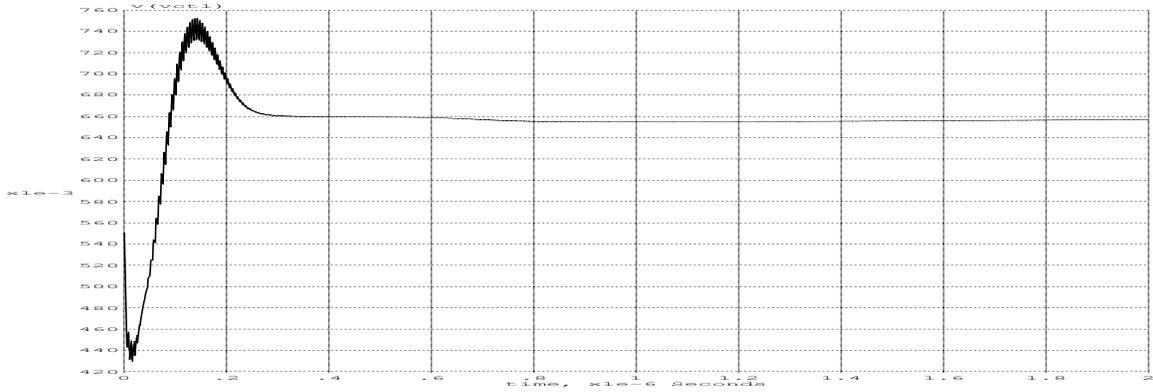


Figure 4-16:  $V_{CTL}$  startup transients as the PLL starts up with 100MHz reference frequency, divide by 16, and the VCO starts up in the correct quadrature mode

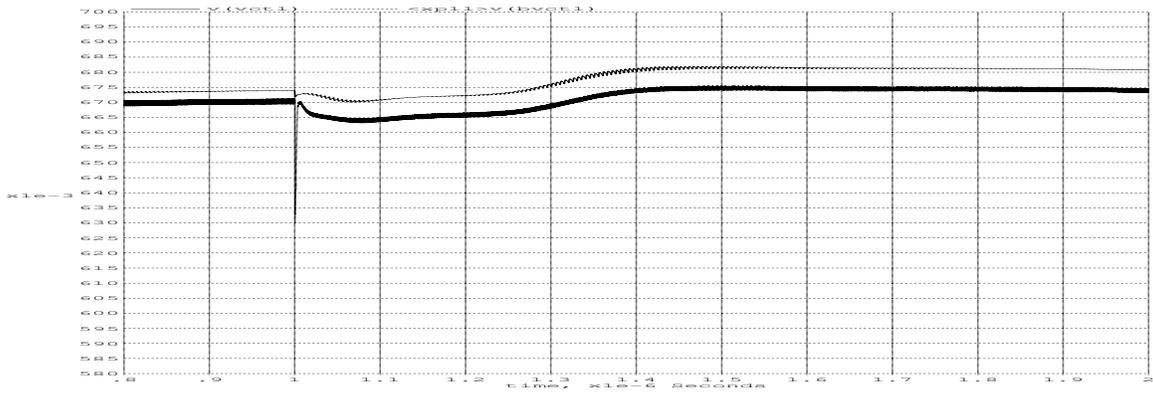


Figure 4-17: PLL response to a step of  $V_{DD}$  by 5% at  $1\mu s$ . The control voltage must go higher in steady-state because the VCO's frequency lowers with a step in voltage supply.

they also lower the  $Q$  of the tank and require more power, adding to greater noise contributions from other sources. While the switches could be made larger, this would add more fixed capacitance to the tank nodes and lower the maximum frequency of the VCO.

The PLL settles as expected across the entire frequency band, coming within 1% of the final control voltage value within 300ns. This number is particularly important because an external controller may need to try many VCO banks until one is found that operates at the correct frequency. This is not as much a problem at the lower frequencies because of the higher overlap between banks, so multiple banks may be

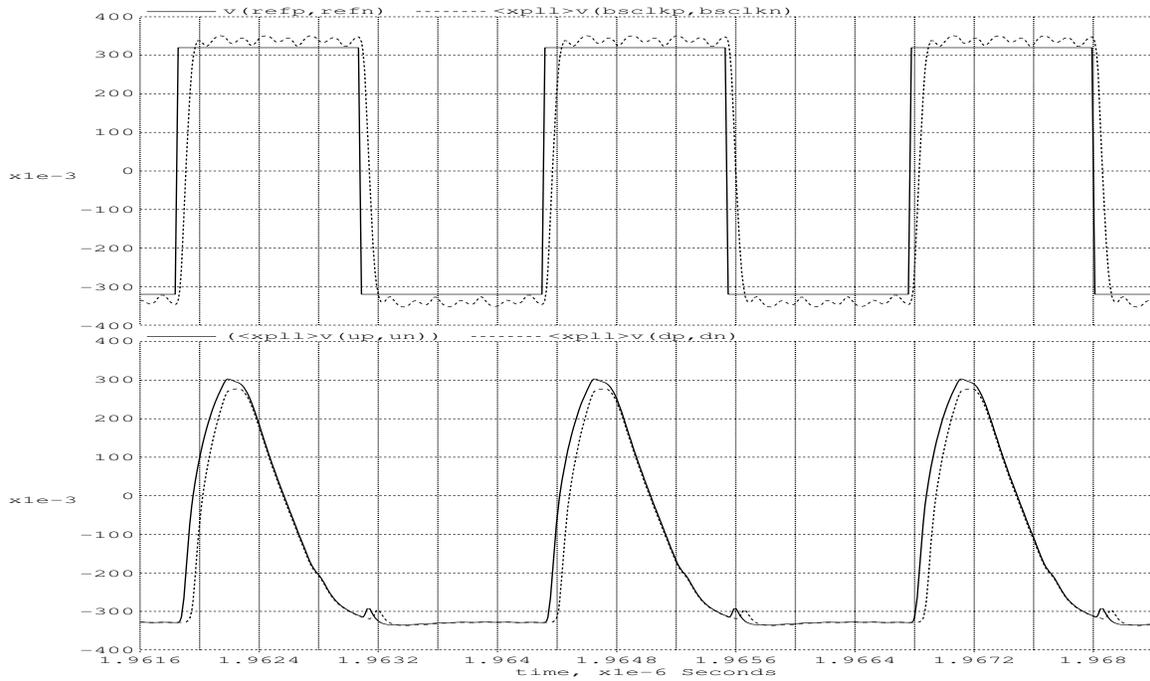


Figure 4-18: Steady-state input and output of the phase-frequency detector, showing the non-zero static phase error

suitable to operate at any given frequency, but at the highest frequencies, only one bank may work.

# Chapter 5

## Conclusion

This chapter summarizes the design and results of the phase-locked loop. It then presents some future extensions using the ideas presented in this thesis.

### 5.1 Design Summary

This thesis presented the design of a phase-locked loop that can provide more flexibility for system integration. Each communication standard has a specific frequency requirement, phase noise specification, and may require quadrature outputs. For systems supporting multiple standards, a monolithic PLL with a wide tuning range, low phase noise, and quadrature outputs, may save significant area and design effort versus using separate PLL's for each supported standard.

The voltage-controlled oscillator is the element in the PLL that has the largest impact on all three of these design targets. It is usually the most limited element in terms of tuning range, is the major contributor to phase noise above the loop bandwidth of the PLL, and is responsible for generating accurate quadrature outputs.

Ring oscillators are capable of much higher tuning ranges than *LC*-VCOs, but their phase noise is much worse. Extra power through a ring oscillator will improve its phase noise performance at the rate of 10dB/decade, but that is usually an unacceptable tradeoff. Therefore, the *LC*-VCO is the basic topology used for the VCO in this thesis.

Digitally switched capacitors are used to make the tuning range of an *LC*-VCO significantly higher than previously published works. When not active, these capacitors add only a small amount of fixed parasitic capacitance to the total capacitance at the tank node. When turned on, though, the center frequency of the VCO is lowered, and analog tuning can be done around this new center frequency. The switches themselves are critical to the performance of the VCO. Smaller switches reduce the amount of parasitic capacitance on the tank node, so the maximum frequency of the VCO can be higher. Larger switches, on the other hand, have less on resistance, so they produce less loss in the tank. The power dissipation is proportional to the amount of loss in the tank, and phase noise is worsened as the tank has more loss, so the switches must be as large as possible with the VCO still able to operate at the highest target frequency of 3.2GHz.

Quadrature outputs are directly generated by the VCO using two cross-coupled cores. A theoretical analysis of this circuit topology is included, including the derivation that the outputs are stable in quadrature. Phase error of the output clocks occurs when the the cores are not identical, such as when the passive components in the resonant tanks are not matched. To understand the effect of this error, a first order model of this error is derived to give the circuit designer an idea of how to set the coupling between the cores to achieve a certain phase error. The quadrature generation uses more than twice the power of just a single VCO core, and it introduces extra noise sources, both detrimental to overall VCO performance.

The quadrature loop has two possible modes of operation, where the outputs of the VCO are  $\pm 90^\circ$  apart. These modes occur at different frequencies, and given sufficient coupling between the nodes, the higher frequency mode is unstable, so the VCO always operates in the same mode. A circuit is developed that forces the VCO into this stable mode in less than 100ns while not wasting current in the coupling circuitry when the VCO is in the correct mode.

The VCO contains two more control loops to stabilize the amplitude and common mode point of its output. The common mode point of the output is set to maximize the tuning range of any capacitor bank, improving overlap between the banks. The

amplitude control loop serves the dual purpose of producing constant amplitude oscillations as well as ensuring that the VCO always has sufficient startup gain. Both of these loops, and an undesired loop formed by interactions between them, are designed to be stable with phase margins near  $45^\circ$ .

The VCO places design constraints on the overall PLL. The control voltage must swing rail-to-rail to ensure adequate overlap between the high frequency banks, and the VCO places a very large capacitive load on this control voltage, which must be buffered.

In addition, the gain of the VCO increases at lower frequencies. To keep the loop dynamics of the PLL roughly constant across frequencies, the charge pump current is adjusted to decrease at lower frequencies to compensate for higher  $K_{VCO}$ . This yields a stable PLL with 1.5MHz bandwidth.

The final VCO's frequency can vary from 1.585-3.254 GHz across all operating conditions, a tuning range of 43%, significantly larger than the Herzel work [2]. This added tuning range comes at the cost of poor phase noise performance at low frequencies. At the highest operating frequency, the phase noise is about 10dBc/Hz lower than at the lowest operating frequency. In fact, the combined phase noise contribution of all the switches at 1.6GHz is greater than the total phase noise at 3.2GHz.

This thesis has met or exceeded all of the original specifications. The inverse relationship between tuning range and phase noise, though, is difficult to overcome, which is why the majority of research goes into very narrowband oscillators. Also, the phase and amplitude errors of the quadrature outputs can be reduced, but only at the expense of added power. These two tradeoffs are what truly limit the ultimate performance of the VCO and PLL.

## 5.2 Future Extensions and Major Contributions

Most PLLs are targeted towards narrowband applications, but sometimes systems need to operate over a much wider frequency range without sacrificing too much noise performance. Small modifications to this thesis can make it extremely suitable

for such systems. One of the primary limitations of the applicability of the PLL is its poor frequency resolution. By changing the divider to one that is capable of more, and larger, division increments, this PLL can use a crystal oscillator as a reference clock and have high frequency resolution of its outputs.

To reduce the phase noise, the technique mentioned in Section 4.2.6 to increase the current through biasing resistors can make an immediate impact. In addition, by reducing the gain of the control loops at lower frequencies, the ISFs of injected noise may similarly decrease. Still, the switches set the limit of the low frequency phase noise, and only reducing the maximum operating frequency will immediately help this.

In summary, this thesis makes three primary contributions. First, it extends the tuning range of an *LC*-VCO by carefully designing a set of switched capacitors that has minimal fixed capacitance so that a high maximum frequency can be reached. Second, the cross-coupled topology to generate quadrature outputs from the VCO is examined for the effect of capacitive mismatch, and a circuit is used to force the VCO into only one of the two possible quadrature modes. Finally, the charge pump is modified so that the PLL can have constant loop dynamics even as the gain of the VCO changes over frequency.

# Appendix A

## Complete Circuit Schematics

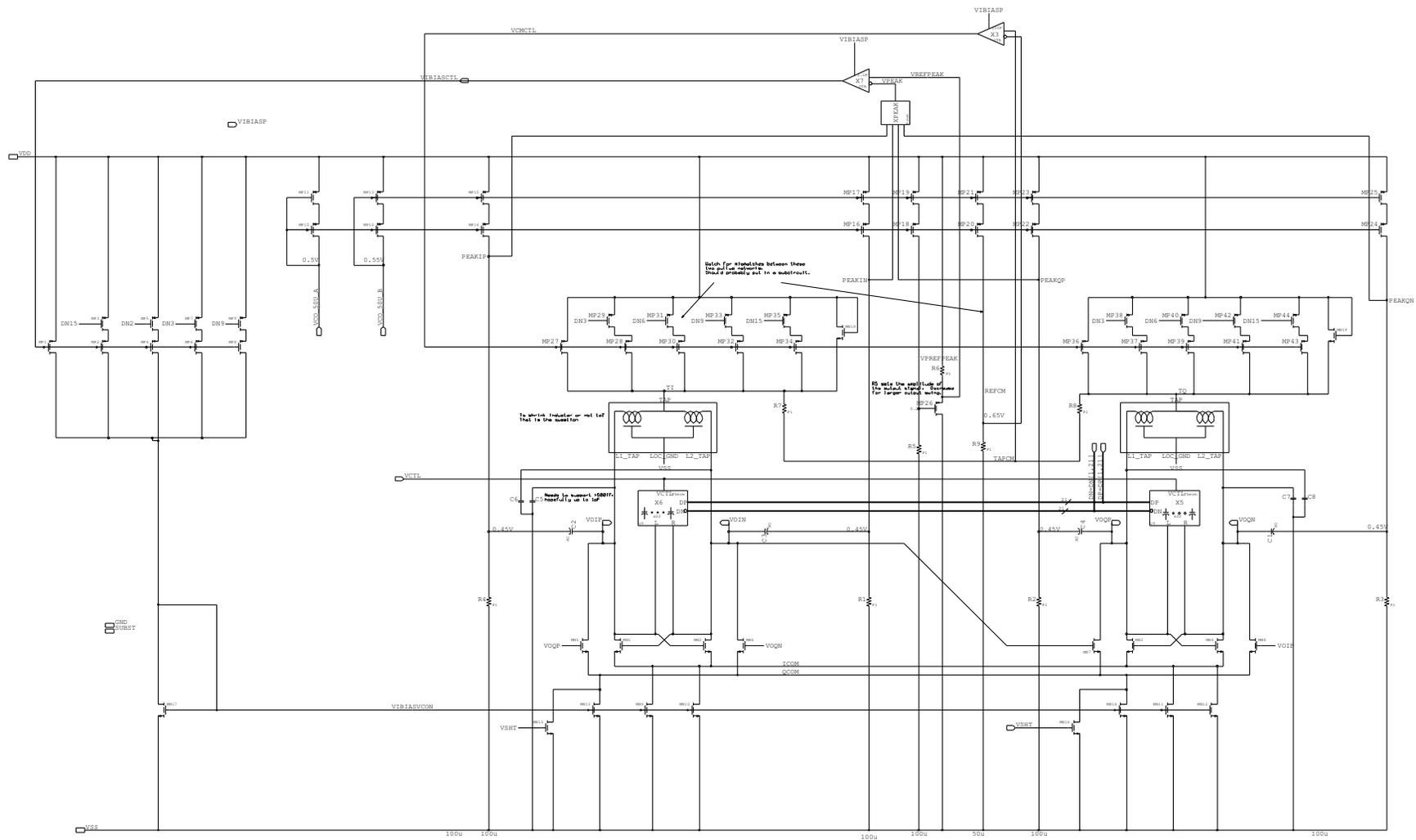


Figure A-1: Complete VCO schematic

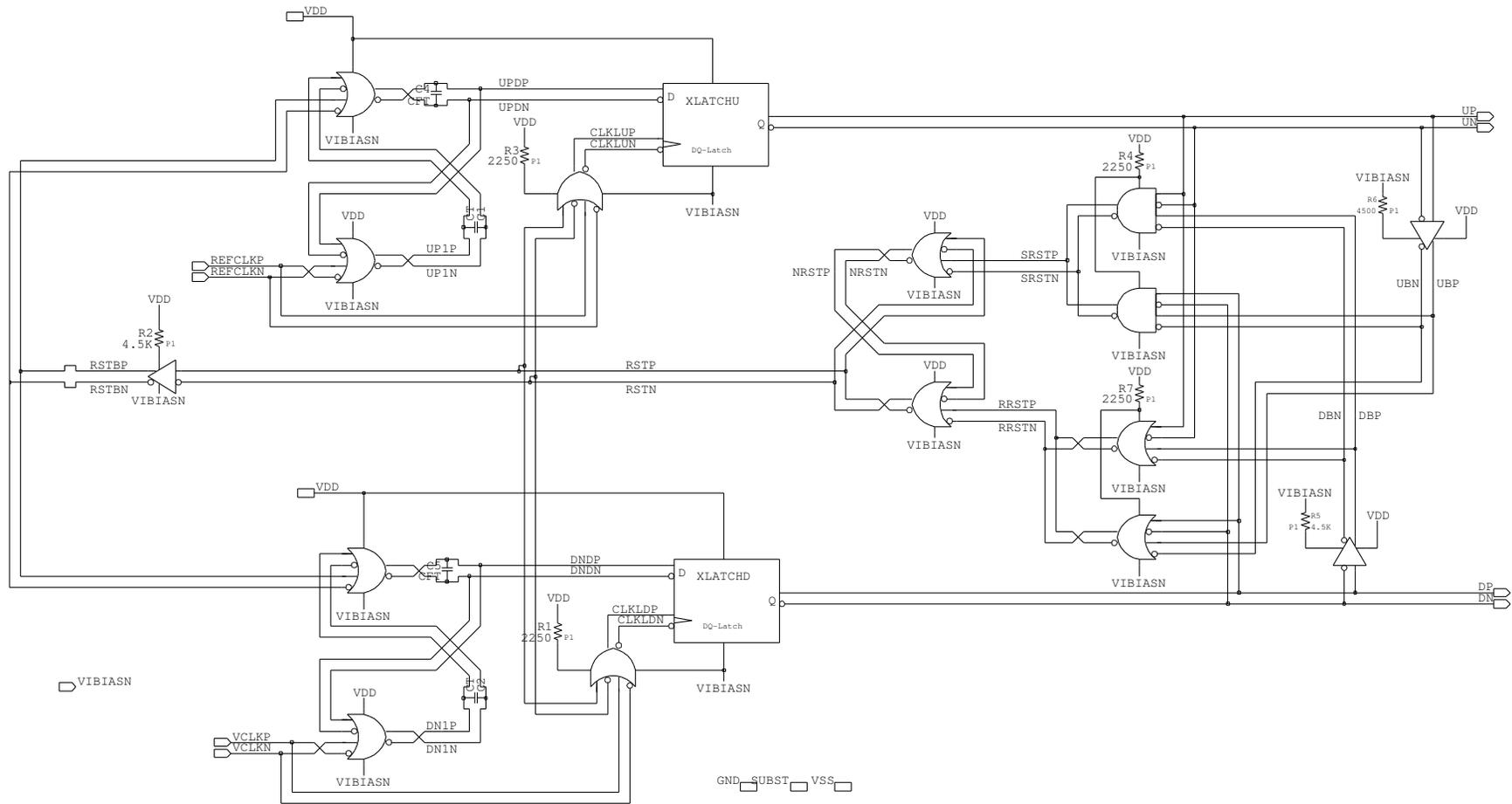


Figure A-2: Modified tristate phase-frequency detector

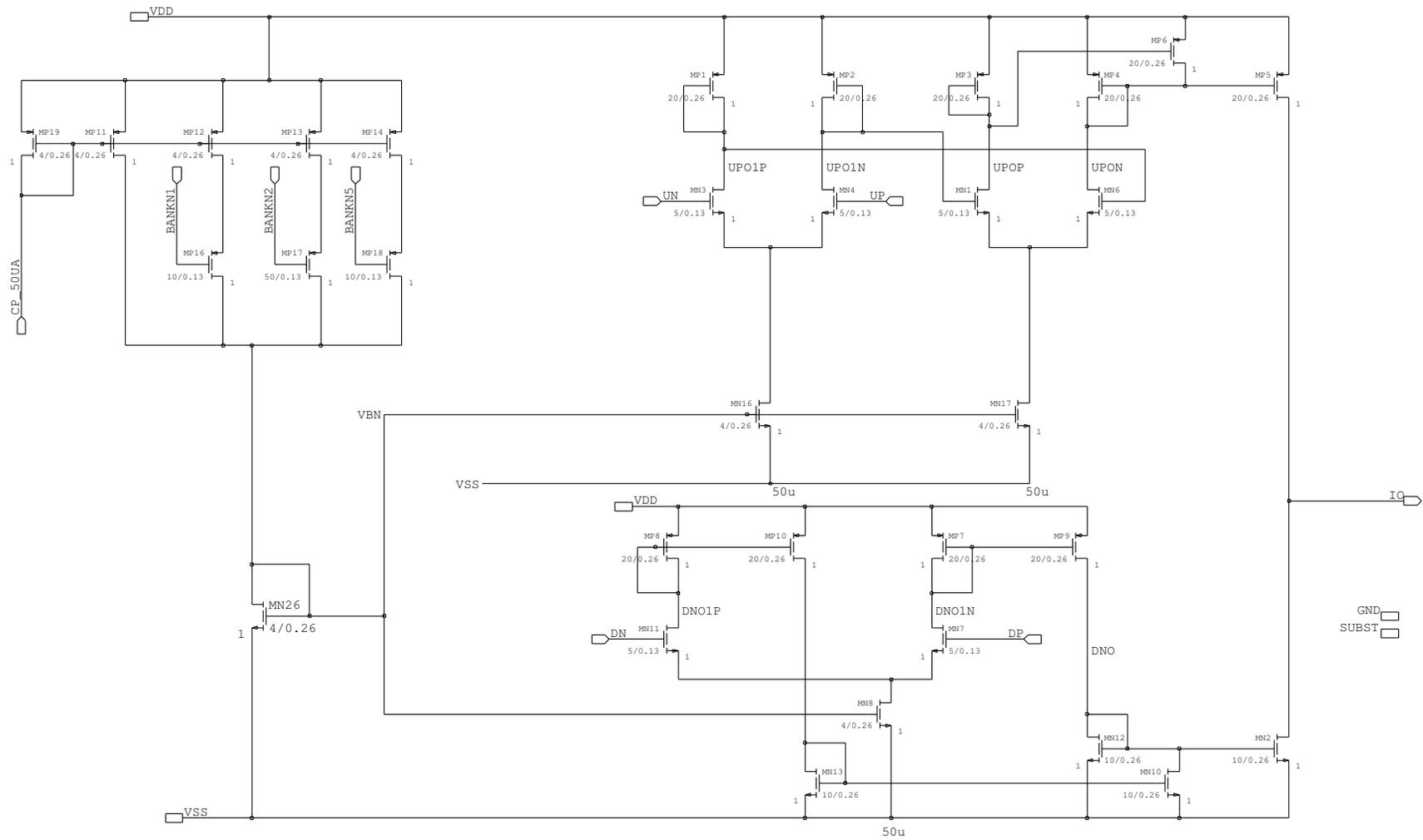


Figure A-3: Charge pump schematic, with compensation for  $K_{VCO}$  variation

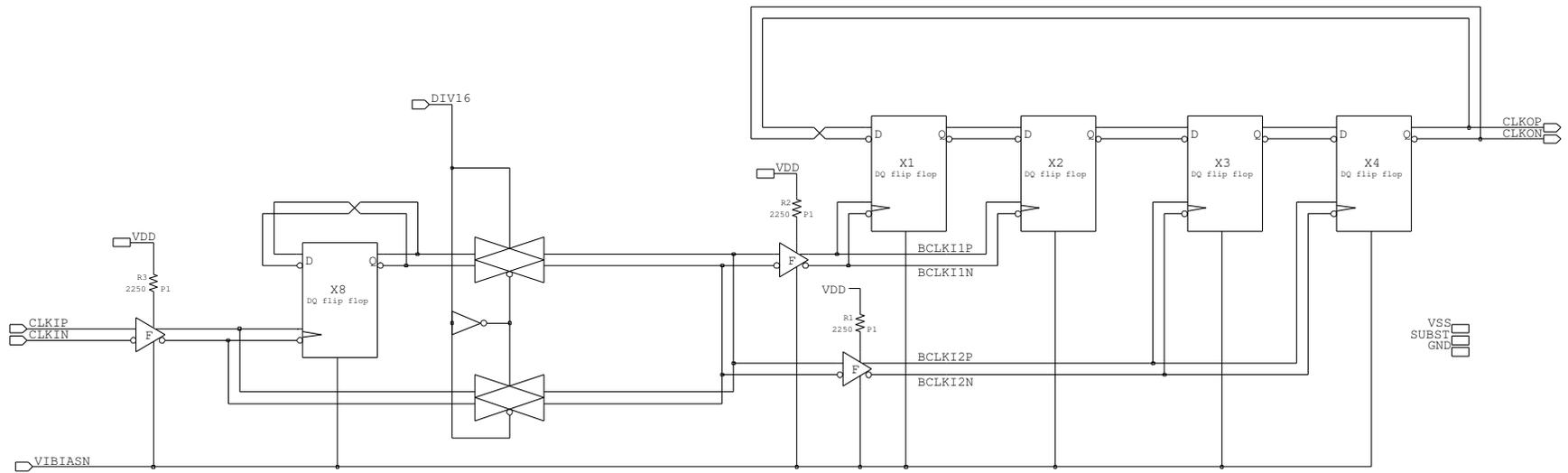


Figure A-4: 8/16 Divider



# Appendix B

## Impulse sensitivity functions

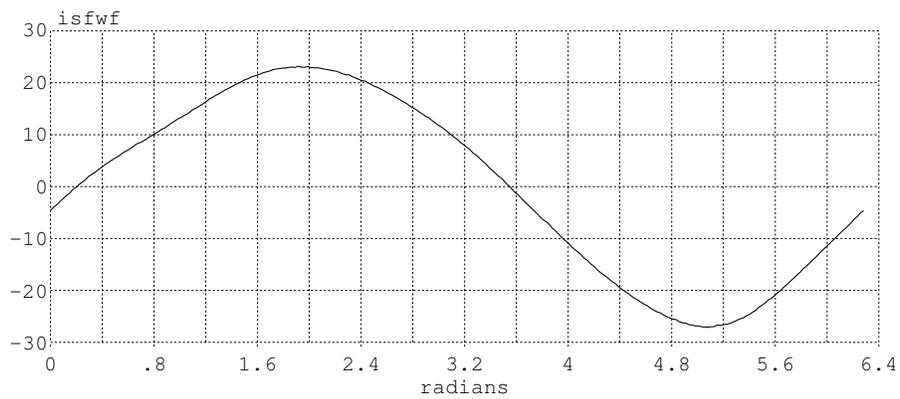


Figure B-1:  $\Gamma(x)/q_{\max}$  for charge injected into  $V_{OQP}$

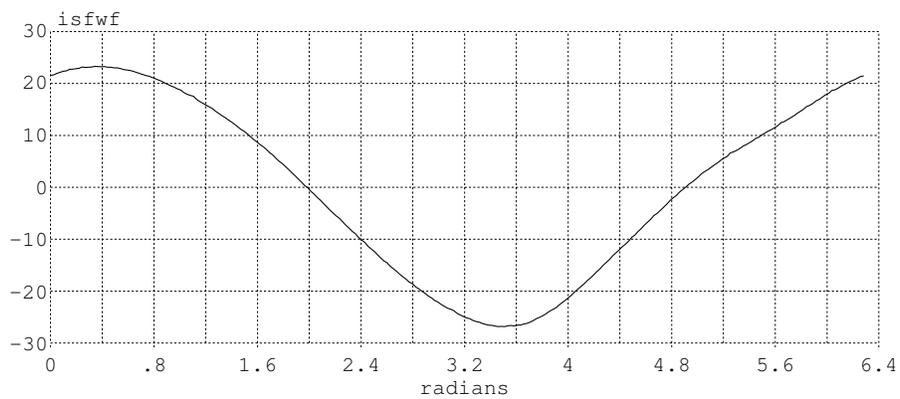


Figure B-2:  $\Gamma(x)/q_{\max}$  for charge injected into  $V_{OIN}$

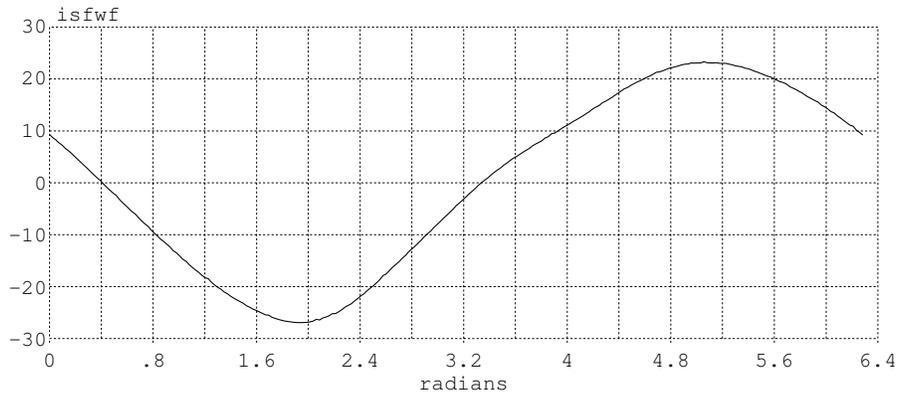


Figure B-3:  $\Gamma(x)/q_{\max}$  for charge injected into  $V_{OQN}$

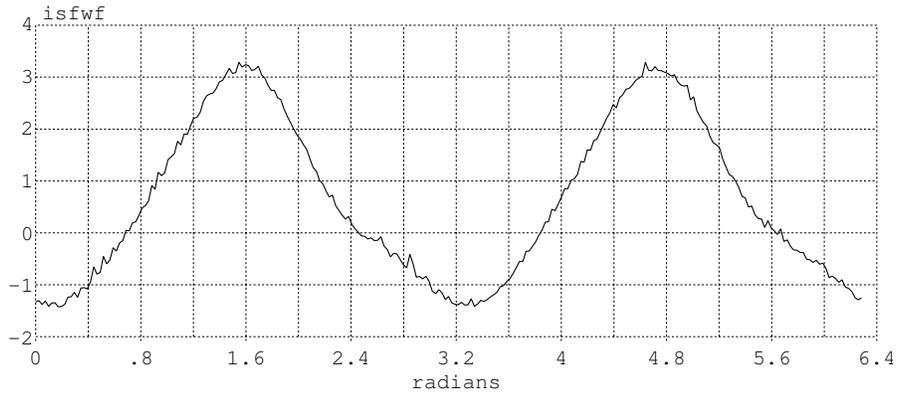


Figure B-4:  $\Gamma(x)/q_{\max}$  for charge injected into  $V_{TI}$

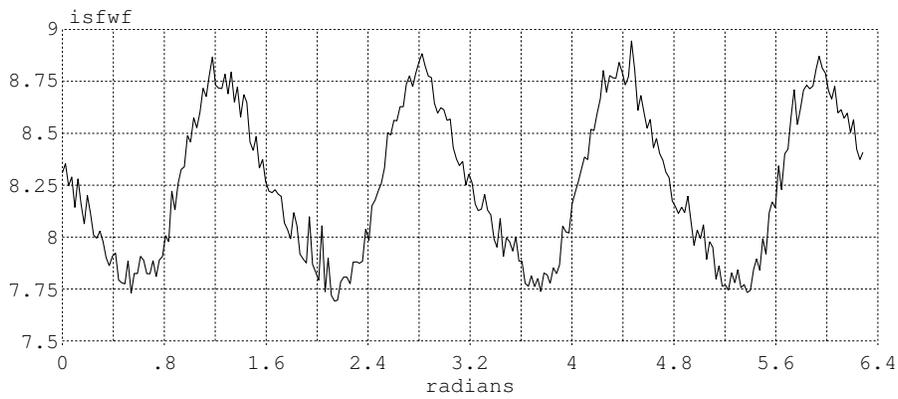


Figure B-5:  $\Gamma(x)/q_{\max}$  for charge injected into  $ICOM$

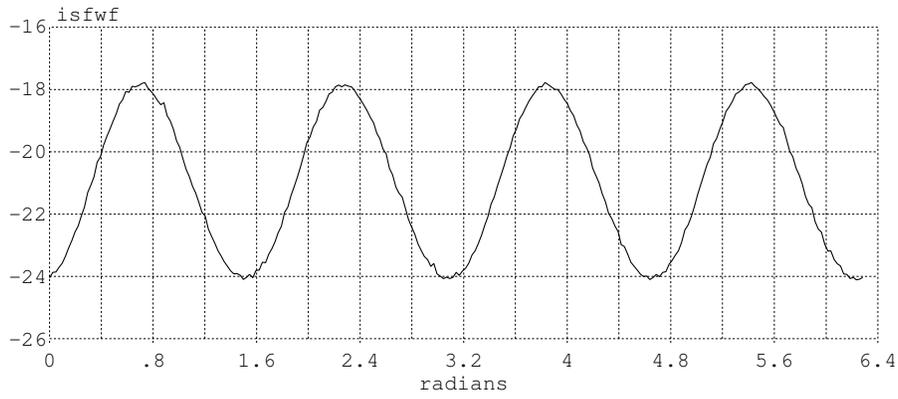


Figure B-6:  $\Gamma(x)/q_{\max}$  for charge injected into  $QCOM$

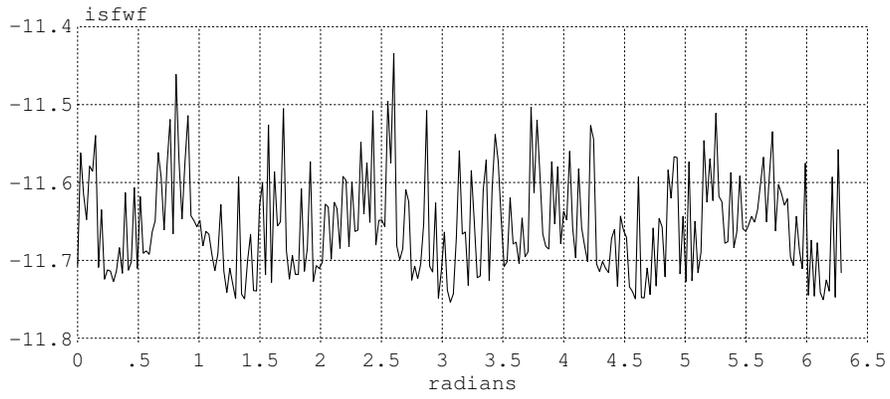


Figure B-7:  $\Gamma(x)/q_{\max}$  for charge injected into  $VCTL$

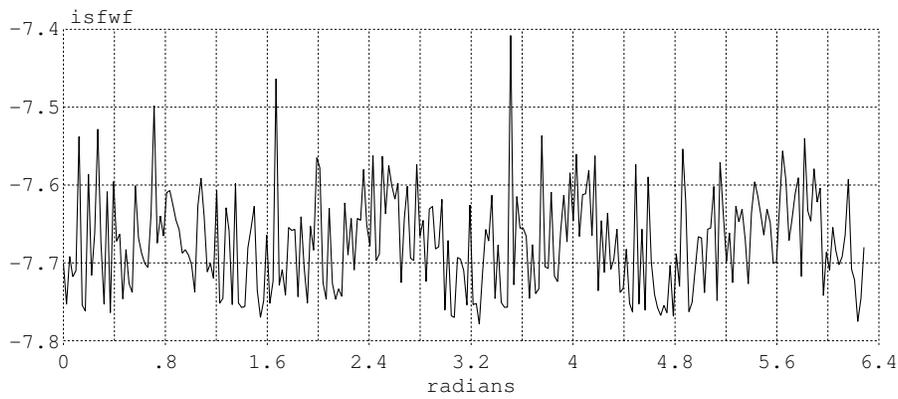


Figure B-8:  $\Gamma(x)/q_{\max}$  for charge injected into  $VBIASCTL$

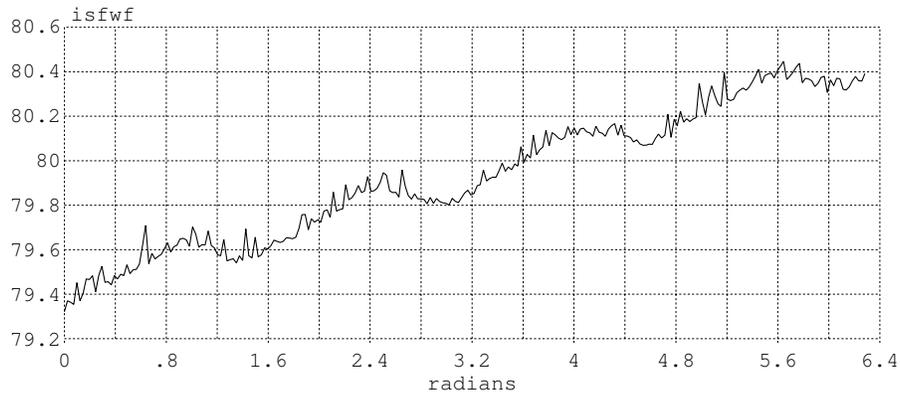


Figure B-9:  $\Gamma(x)/q_{\max}$  for charge injected into  $V_{REFCM}$

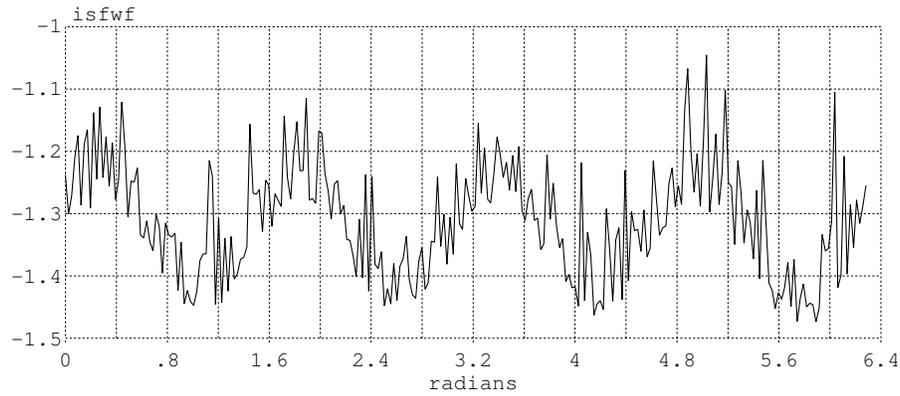


Figure B-10:  $\Gamma(x)/q_{\max}$  for charge injected into  $V_{CMCTL}$

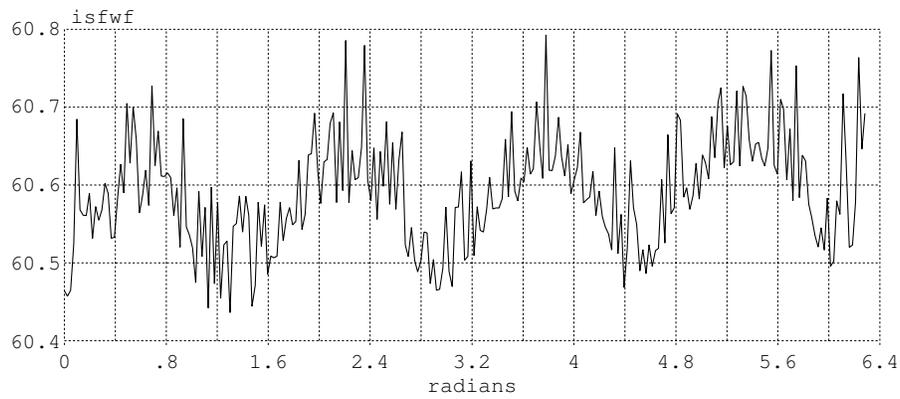


Figure B-11:  $\Gamma(x)/q_{\max}$  for charge injected into  $V_{PEAK}$

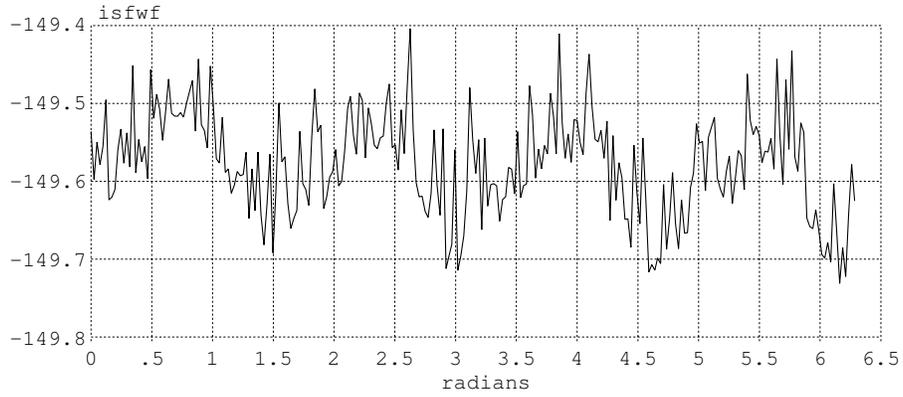


Figure B-12:  $\Gamma(x)/q_{\max}$  for charge injected into  $V_{REFPEAK}$

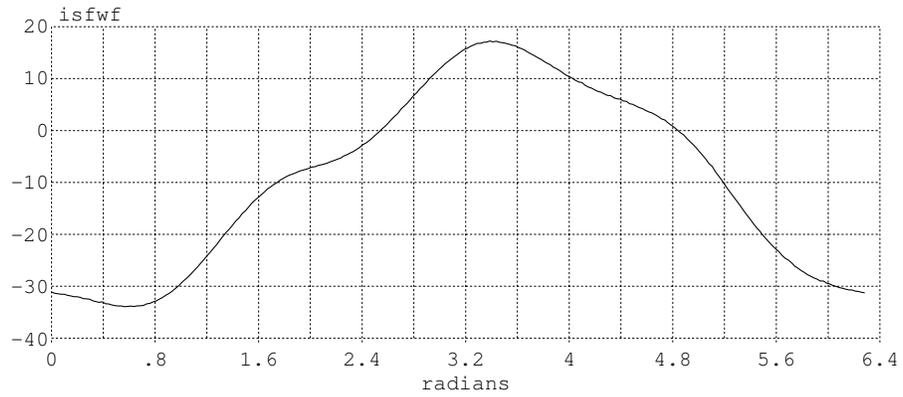


Figure B-13:  $\Gamma(x)/q_{\max}$  for charge injected parallel to the drain current referred noise of  $M_{N1}$

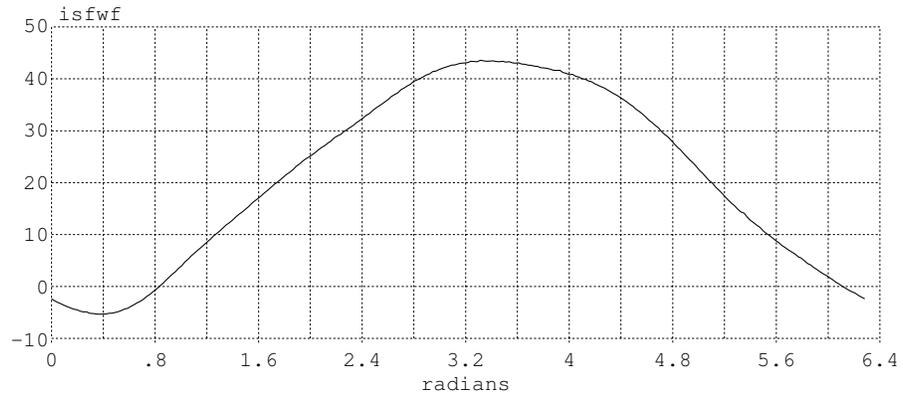


Figure B-14:  $\Gamma(x)/q_{\max}$  for charge injected parallel to the drain current referred noise of  $M_{N5}$

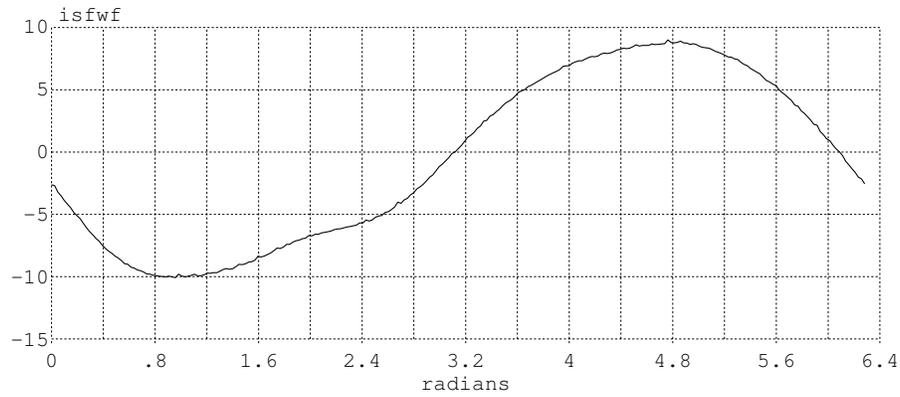


Figure B-15:  $\Gamma(x)/q_{\max}$  for charge injected parallel to the transmission gates in any of the capacitor banks

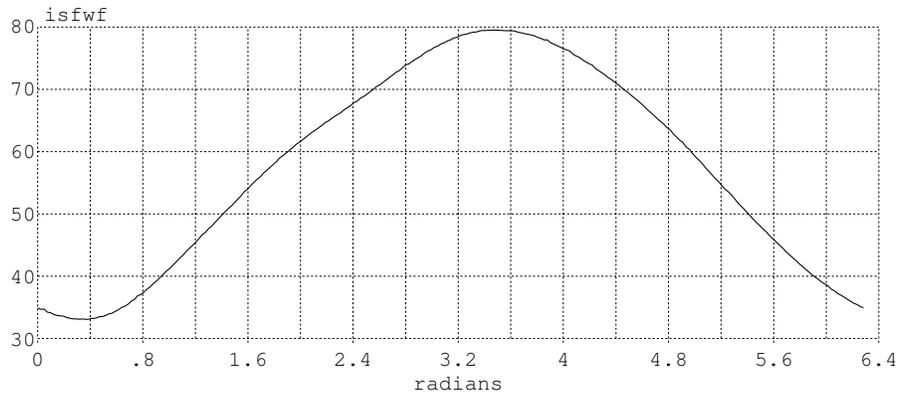


Figure B-16:  $\Gamma(x)/q_{\max}$  for charge injected at the peak detector's input

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