

A 19-bit Monolithic Charge-Balancing A/D Converter

by

Tung Shen Chew

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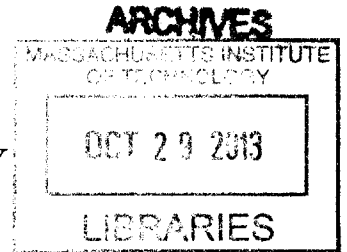
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Abstract

Existing high-resolution ADC topologies are expensive, complicated and vulnerable to switch leakage at high temperature. This thesis introduces the Modified Landsburg ADC, a high-resolution converter optimized for minimum cost and die area. Switch resistance cancellation, charge-injection compensation and auto-zero methods are used to build a simple and robust ADC which will operate reliably across the military temperature range. Implemented on a $0.25\mu\text{m}$ CMOS process, with a die area of under 300mil^2 , the Modified Landsburg ADC achieves an ENOB of 15.6 bits and an SNR of 95.8dB at 5 Samples/s while consuming $<2\text{mW}$. It enables the integration of a high-resolution converter in smaller, cheaper systems.

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Chapter 1

Introduction

1.1 Project Motivation

Analog-to-digital converters (ADCs) act as an essential interface between the continuous, analog signals of the real world and the discretized signals which can be processed by digital electronics. Multiple ADC architectures remain popular over time because each one represents a specific compromise between speed, power, resolution and cost. Depending on the requirements of an application, some architectures are more suitable than others.

Many applications exist which require high resolution (>16 bits) at near-DC bandwidth ($<10\text{Hz}$), such as handheld multimeters and temperature gauges. Historically, the architecture of choice for such applications has been the dual-slope ADC, which has since fallen out of favor due to the semiconductor industry's trend towards low-voltage, fully-integrated, single-supply circuits. This is incompatible with the dual-slope architecture's need for a fairly high supply voltage and large external capacitors. Table 1.1 shows four high-resolution commercial ADCs released in the last decade[1][2][3][4], whereas Table 1.2 shows a few¹ recent academic high-resolution designs[5][6][7]. The discrete-time sigma-delta (DT $\Sigma\Delta$) architecture is clearly dominant among high-resolution designs.

¹Very few examples are available, as recent academic ADC research is much more focused on high bandwidth than high resolution.

Table 1.1: Commercially available high-resolution, low-bandwidth ADCs

Product	ISL26132	LTC2482	MCP3425	CS5526
Manufacturer	Intersil	Linear Tech	Microchip	Cirrus Logic
Year	2011	2005	2007	2005
Architecture	DT $\Sigma\Delta$	DT $\Sigma\Delta$	DT $\Sigma\Delta$	DT $\Sigma\Delta$
Resolution (bits)	24	16	16	20
Sample Rate (Samples/s)	10-80	6.8	15	15
INL error (ppm of FSR)	3 at 25 °C 10 over temp	2 at 25 °C 20 over temp	10 at 25 °C	7 at 25 °C 15 over temp
Approximate SNDR (dB)	111	97.5	97.5	109
Supply Current	10mA	160 μ A	155 μ A	1.65mA

Table 1.2: Academic high-resolution, low-bandwidth ADCs

Author	J. E. Johnston	C. B. Wang	V. Quiquemmpoix
Year	1999	2000	2006
Architecture	DT $\Sigma\Delta$	DT $\Sigma\Delta$	DT $\Sigma\Delta$
Resolution (bits)	24	20	22
Sample Rate (Samples/s)	7.5	25k	15
INL error (ppm of FSR)	3 at 25 °C	12 at 25 °C	4 at 25 °C
Approximate SNDR (dB)	110	98	108
Supply Current	-	15mA	120 μ A

There are several reasons why the DT $\Sigma\Delta$ architecture works poorly at high-resolution. High-resolution DT $\Sigma\Delta$ ADCs require large switching capacitors to reduce $\frac{kT}{C}$ sampling noise to sub-LSB levels and minimize charge injection nonlinearity (caused by the unpredictable number of switching transitions). These large capacitors must be driven by an input buffer. The large capacitors and input buffer raise the cost of the ADC, which is further increased by the need for an anti-aliasing input filter. Finally, linearity cannot be maintained at high temperature due to switch leakage. These fundamental limitations indicate a need for a different ADC architecture, tailored specifically for this role.

This paper describes a charge-balancing ADC which achieves high-resolution, low-bandwidth performance at minimal cost. It is based on an architecture introduced by George Landsburg in 1977 [8] (hereafter referred to as the Landsburg architecture). The proposed changes to the architecture have focused on leveraging the advantages of

modern silicon and meeting contemporary expectations of an ADC². The Landsburg has been modified to run at a much higher resolution³, run off of a single 3-5V supply and require no external components. Full use is made of the speed and inexpensive digital logic of the modern 0.25 μ m process.

1.2 Organization of Thesis

Chapter 1 introduces the central problem of the thesis.

Chapter 2 is a thorough description of the original Landsburg ADC. It is described in terms of its similarity to the dual-slope and continuous-time $\Sigma\Delta$ topologies.

Chapter 3 outlines the proposed architectural changes to match the Landsburg ADC with modern needs and manufacturing capabilities. In-depth analysis is done on the advantages and trade-offs of each modification.

Chapter 4 describes the various analog subsystems in the ADC: the input switch network & amplifier, up/down current source, integrating amplifier and latching comparator. This chapter details the function, specifications and transistor-level implementation of each of these blocks.

Chapter 5 details how noise sources inside the ADC affect its output.

Chapter 6 concludes the thesis and suggests a direction for future work.

²To the extent of the author's knowledge, this is the first time this architecture has been used since Landsburg's original work.

³19 bits, as opposed to the original 12 bits.

Chapter 2

The Landsburg ADC

2.1 Limitations of the Dual-Slope and CT $\Sigma\Delta$ ADC

As little work has been done on the Landsburg ADC since its conception, this thesis will include a full description of its operation. We will first review two common low-bandwidth, high-resolution ADC topologies: the dual-slope ADC and the Continuous-Time Sigma-Delta (CT $\Sigma\Delta$) ADC. They both work on the following principle:

1. Charge is added to a capacitor in a quantity (Q_1) controlled by the input voltage.
2. A measured quantity of charge (Q_2) is drained from the capacitor until the charge added in step 1 has been precisely removed.
3. $Q_1 + Q_2 \equiv 0$, so by measuring Q_2 , we measure Q_1 and hence the input voltage.

2.1.1 The Dual-Slope ADC

Figure 2-1 illustrates the dual-slope ADC, which is composed of an integrator, a comparator and an input switch, S_{in} . As shown in Figure 2-2, the dual-slope ADC executes steps 1 and 2 sequentially to perform a conversion. The integration capacitor's voltage is initially at the comparator's threshold. In step 1, the integrator integrates a current proportional to the input voltage for a fixed amount of time (t_{up}). At the end of t_{up} , an additional voltage (and charge) proportional to the input voltage

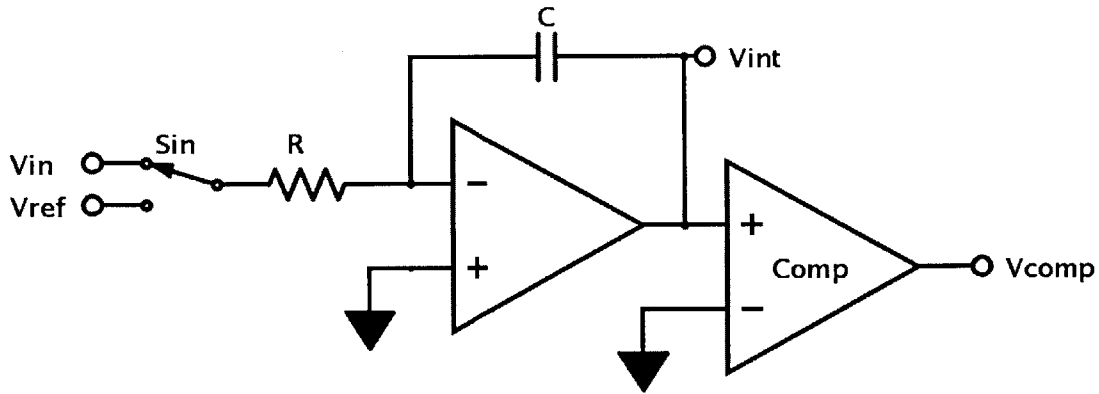


Figure 2-1: The Dual-Slope ADC

has been stored on the integration capacitor. Charge added in step 1:

$$Q_1 = i_{in} t_{up} = \frac{v_{in} t_{up}}{R}$$

In step 2, the integration capacitor is discharged at a fixed rate set by the reference voltage. The comparator flips after an additional duration of t_{down} , when the added charge from step 1 has been fully removed in step 2. Charge added in step 2:

$$Q_2 = i_{ref} t_{down} = \frac{v_{ref} t_{down}}{R}$$

The more charge which has been added in step 1, the more time required to remove that charge in step 2. This results in a measurement of v_{in} :

$$Q_1 + Q_2 = 0$$

$$v_{in} = -v_{ref} \frac{t_{down}}{t_{up}}$$

For a clocked system, rewriting $t_x = n_x t_{clock}$:

$$v_{in} = -v_{ref} \frac{n_{down}}{n_{up}}$$

While the dual-slope is a simple topology capable of very high resolution, it has

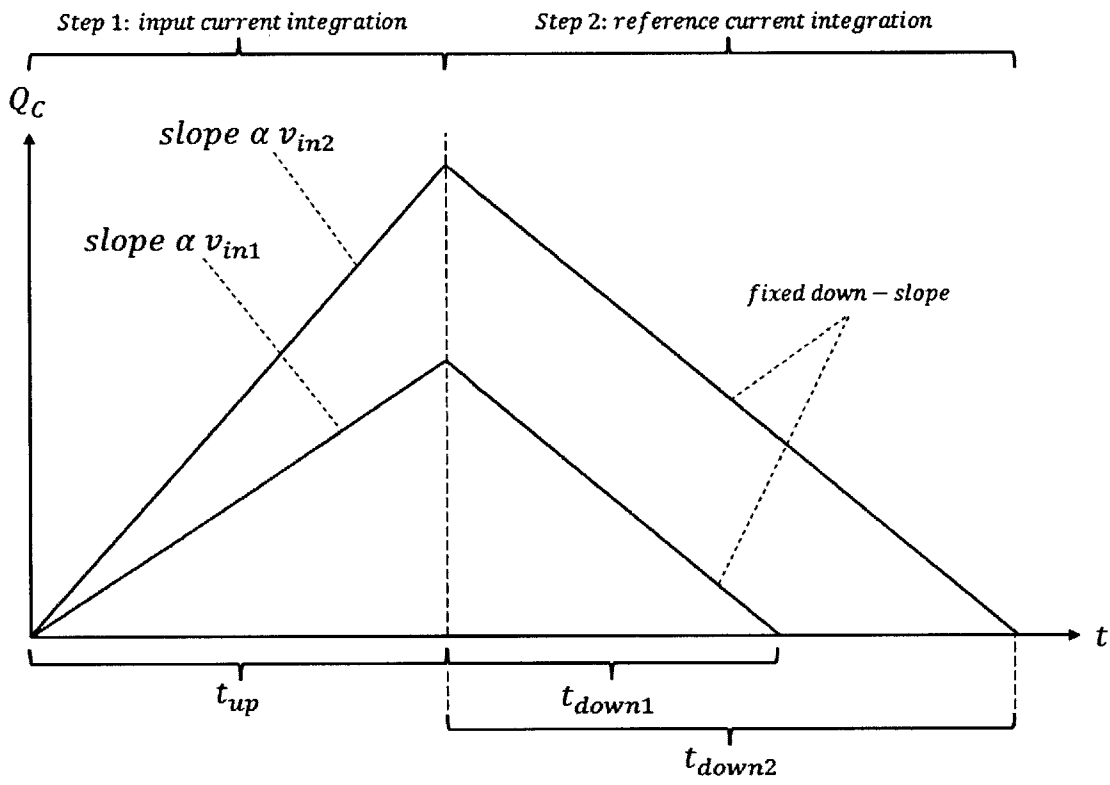


Figure 2-2: Charge on dual-slope integration capacitor

several major disadvantages.

Firstly, the ADC's output is derived from the timing of a single, extremely precise comparator decision, which places harsh requirements on the speed, accuracy and noise performance of the comparator. This is because the ADC performs steps 1 and 2 sequentially, adding and then removing charge. At the end of step 1, substantial charge - and high voltage - accumulates on the integrating capacitor. This is the high tip of the triangle in Figure 2-2, which may be over 100V in precision designs. This substantial instantaneous charge requires that the integration capacitor be an expensive external component with a very low voltage coefficient, increasing the bill-of-materials and circuit board area required to use the ADC.

The comparator requirements are relaxed if the integrator is allowed to swing over a relatively large voltage, allowing for faster, more decisive comparator transitions. Nevertheless, this requires a high supply voltage which is incompatible with modern, low-voltage manufacturing processes. For these reasons, the dual-slope ADC has fallen out of mainstream use.

2.1.2 The Continuous Time $\Sigma\Delta$ ADC

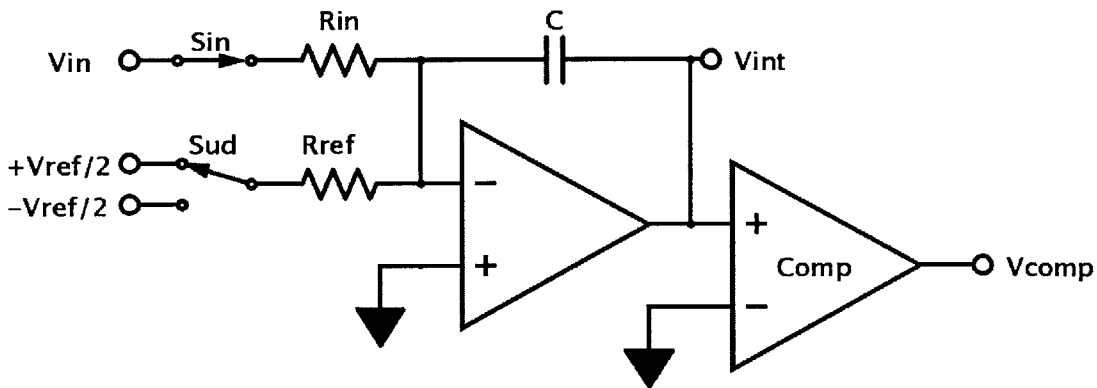


Figure 2-3: The CT $\Sigma\Delta$ ADC

The CT $\Sigma\Delta$ topology, illustrated in Figure 2-3, differs from the dual-slope by performing steps 1 and 2 simultaneously. The ADC integrates a current proportional to v_{in} for a fixed number of clock cycles. At the beginning of every clock cycle, a

decision is made to move the up-down switch, S_{ud} to either $+\frac{1}{2}v_{ref}$ or $-\frac{1}{2}v_{ref}$. Over the duration of that clock cycle, this either adds or subtracts a charge $\Delta Q = \frac{v_{ref}t_{clock}}{2R_{ref}}$. This decision is made to drive the integrated charge towards zero; if $Q_{int} < 0$, charge is added, and if $Q_{int} > 0$, charge is subtracted. The resulting (simplified) charge waveform is shown in Figure 2-4 for a total of 10 clock cycles. The top dotted line shows the total charge added by the input voltage (Q_1) and the bottom dotted line shows the total charge added by successive integrations of $\pm\frac{1}{2}v_{ref}$ (Q_2). The solid line is the sum of these two charges.

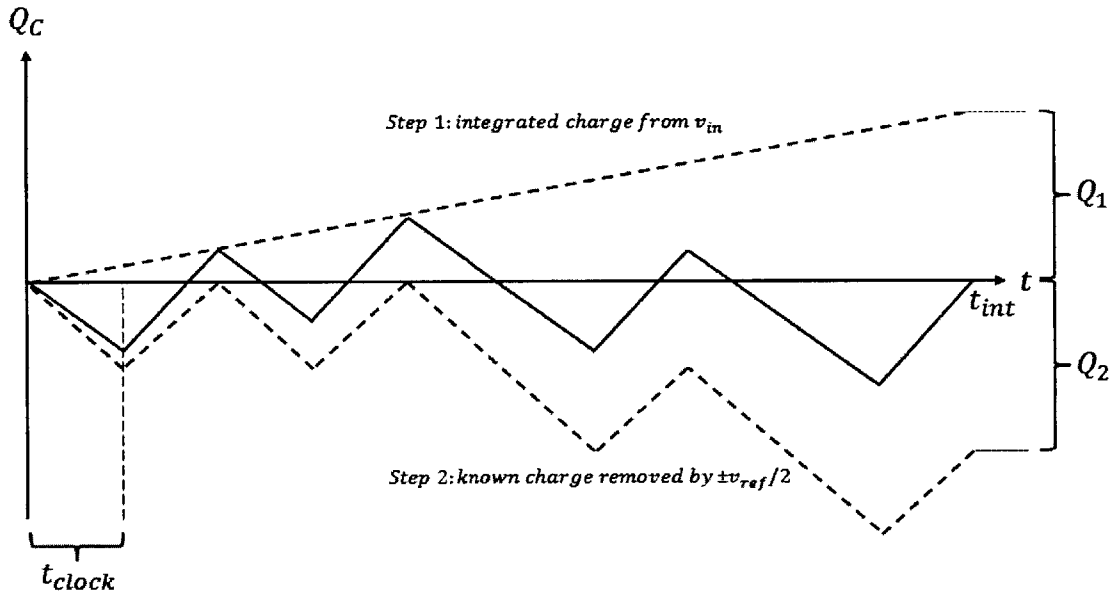


Figure 2-4: Charge on CT $\Sigma\Delta$ ADC integration capacitor

Assuming that charge is added for n_{add} cycles and charge is subtracted for $n_{subtract}$ cycles, the total charge contributed by step 2 is:

$$Q_2 = \frac{v_{ref}t_{clock}}{2R_{ref}}(n_{add} - n_{subtract})$$

Hence we can find v_{in} as a function of n_{add} and $n_{subtract}$:

$$Q_1 = i_{in}t_{up} = \frac{v_{in}t_{clock}}{R_{in}}(n_{add} + n_{subtract})$$

$$Q_1 + Q_2 = 0$$

$$v_{in} = v_{ref} \frac{R_{in}}{2R_{ref}} \frac{n_{subtract} - n_{add}}{n_{subtract} + n_{add}}$$

In the example in Figure 2-4, with $n_{add} = 4$ and $n_{subtract} = 6$:

$$v_{in} = v_{ref} \frac{R_{in}}{2R_{ref}} \frac{6 - 4}{6 + 4}$$

As long as $|\frac{v_{in}}{R_{in}}| < |\frac{v_{ref}}{2R}|$, the negative feedback action will always limit the integrated charge to within $\pm(|\frac{v_{in}}{R_{in}}| + |\frac{v_{ref}}{2R_{ref}}|)t_{clock}$. In other words, by performing steps 1 and 2 simultaneously (adding and subtracting charge simultaneously) we manage to drastically reduce the peak charge and voltage on the capacitor. This circumvents several problems with the dual-slope ADC: a small, on-chip integrating capacitor can be used and the ADC can be implemented on a low-voltage manufacturing process. Demands on comparator performance are greatly reduced, as the ADC output is no longer derived from a single, precise comparator decision. Instead it is a result of many decisions, one every clock cycle, where the comparator is triggered off of a much larger, faster waveform.

Nevertheless, the CT $\Sigma\Delta$ ADC has a source of nonlinearity which compromises its use for high-resolution conversion. Every clock cycle, S_{ud} is set to either $+\frac{1}{2}v_{ref}$ or $-\frac{1}{2}v_{ref}$. During each transition between $+\frac{1}{2}v_{ref}$ and $-\frac{1}{2}v_{ref}$, charge is injected from S_{ud} into the integrating capacitor. As the number of switch transitions is unpredictable, this ill-defined number of charge injections appears as noise and nonlinearity at the CT $\Sigma\Delta$ ADC's output[10]. High-resolution $\Sigma\Delta$ ADCs are still built in spite of this effect, albeit with several engineering workarounds. These include the use of bigger capacitors, higher integration currents and larger switches with carefully balanced positive and negative charge injections. As these workarounds do not scale well to a small, low-cost design, the following section will offer a method to lock the number of switch transitions.

2.2 Introducing the Landsburg ADC

2.2.1 Locking the Number of Switch Transitions

This section describes a return-to-zero method which fixes the number of switch transitions to improve the linearity of the CT $\Sigma\Delta$ ADC. If the number of switch transitions (and hence the quantity of charge injection) is constant for each measurement, this charge injection results in input offset instead of nonlinearity and noise. This offset can then be removed using zero-offset calibration techniques, to be discussed in Chapter 2.2.3.

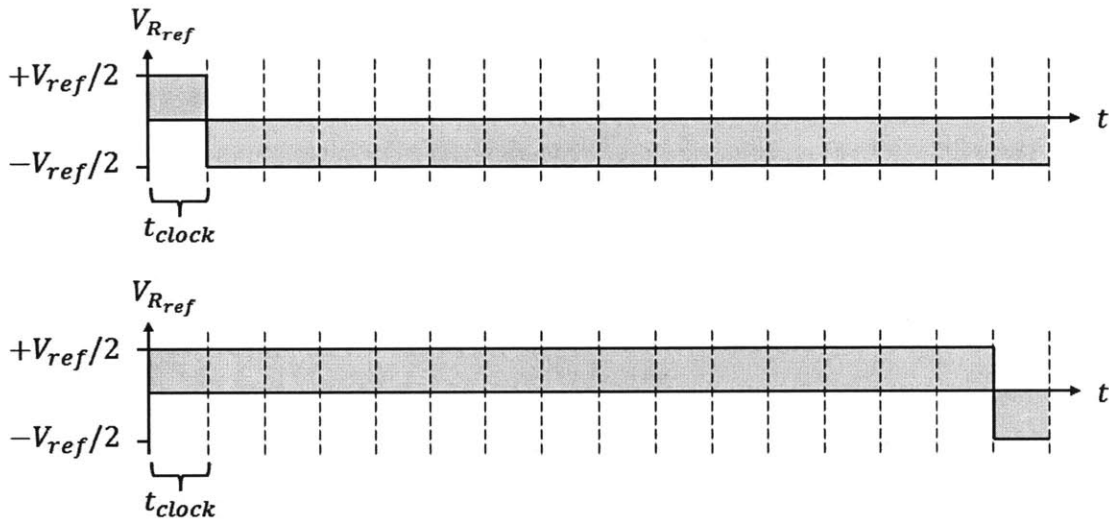


Figure 2-5: Landsburg ADC 16-clock switching sequences: low (upper) & high (lower)

Previously, a decision was made to set S_{ud} to $+\frac{1}{2}v_{ref}$ or $-\frac{1}{2}v_{ref}$ at the start of every clock cycle. Consider a system where this decision is made every 16 clock cycles instead, and sets the $+\frac{1}{2}v_{ref}$ or $-\frac{1}{2}v_{ref}$ pattern for the next 16 cycles. In order to force one $+\frac{1}{2}v_{ref}$ to $-\frac{1}{2}v_{ref}$ transition and one $-\frac{1}{2}v_{ref}$ to $+\frac{1}{2}v_{ref}$ transition, the 16-clock sequences in Figure 2-5 are used. The first cycle in each sequence is always high and the last cycle in each sequence is always low, so one transition in each direction must occur. As the charge from the first cycle cancels out the charge from the last cycle, the high and low sequences add or subtract 14 cycles of charge from the integrating capacitor. Hence, denoting the number of high and low sequences as

N_{high} and N_{low} respectively, v_{in} can be found:

$$\begin{aligned}
Q_1 &= i_{in} t_{up} = \frac{v_{in} t_{clock}}{R_{in}} 16(N_{high} + N_{low}) \\
Q_2 &= \frac{v_{ref} t_{clock}}{2R_{ref}} 14(N_{high} - N_{low}) \\
Q_1 + Q_2 &= 0 \\
v_{in} &= v_{ref} \frac{R_{in}}{2R_{ref}} \frac{14(N_{low} - N_{high})}{16(N_{low} + N_{high})}
\end{aligned}$$

Defining the total integration time, $t_{integration} = t_{clock} n_{integration} = 16t_{clock} N_{integration}$, where $N_{integration} = \frac{1}{16} n_{integration} = N_{high} + N_{low}$:

$$v_{in} = v_{ref} \frac{R_{in}}{2R_{ref}} \frac{14(2N_{low} - N_{integration})}{16N_{integration}}$$

While this system has improved linearity over the CT $\Sigma\Delta$ ADC, it requires a much faster clock. If each 16-clock pattern represents one count, a clock with $16\times$ frequency will be needed, compared to a CT $\Sigma\Delta$ ADC of equal resolution.

What if we define a single-clock charge difference to be one count, and we add an additional mechanism to measure single-clock charge differences? Then each 16-clock pattern represents 14 counts, and we only need a clock with $\frac{16}{14}\times$ frequency, compared to a CT $\Sigma\Delta$ ADC of equal resolution. The next section will explain how this is implemented in the Landsburg architecture.

2.2.2 Discerning One-Clock Charge Differences

Defining d_{out} as the digital output code:

$$d_{out} = \lfloor d_{out}/14 \rfloor + d_{out} \bmod 14$$

where we have only been able to discern the $\lfloor d_{out}/14 \rfloor$ term. The remainder, $d_{out} \bmod 14$ comes from the residual charge on the integrating capacitor at the end of the conversion, which should be in the range of $\pm 14 \frac{v_{ref}}{2R_{ref}} t_{clock}$. In order to measure this charge,

the Landsburg behaves like a 5-bit dual-slope converter. Figure 2-6 illustrates this behavior for two example values of residual charge, Q_{res1} and Q_{res2} . In both cases, after n_{int} 16-cycle-sequence integration cycles, S_{in} is opened to halt any further current from v_{in} and preserve the residual charge on the integrating capacitor. S_{ud} is then set to $-\frac{1}{2}v_{ref}$ to integrate up for a fixed number of cycles (n_{up}). This ensures that $Q_c > 0$ before the final down-integration. Finally, as in the dual-slope ADC, the integration capacitor is discharged at a fixed rate (by setting S_{ud} to $+\frac{1}{2}v_{ref}$) until an up-to-down comparator transition occurs. The number of clock cycles which elapse before the comparator transition (n_{down}) indicate how much residual charge remained. The entire conversion can be summarized with the formula:

$$v_{in} = v_{ref} \frac{R_{in}}{2R_{ref}} \left(\frac{14(2N_{low} - N_{integration}) + n_{down} - n_{up}}{16N_{integration}} \right)$$

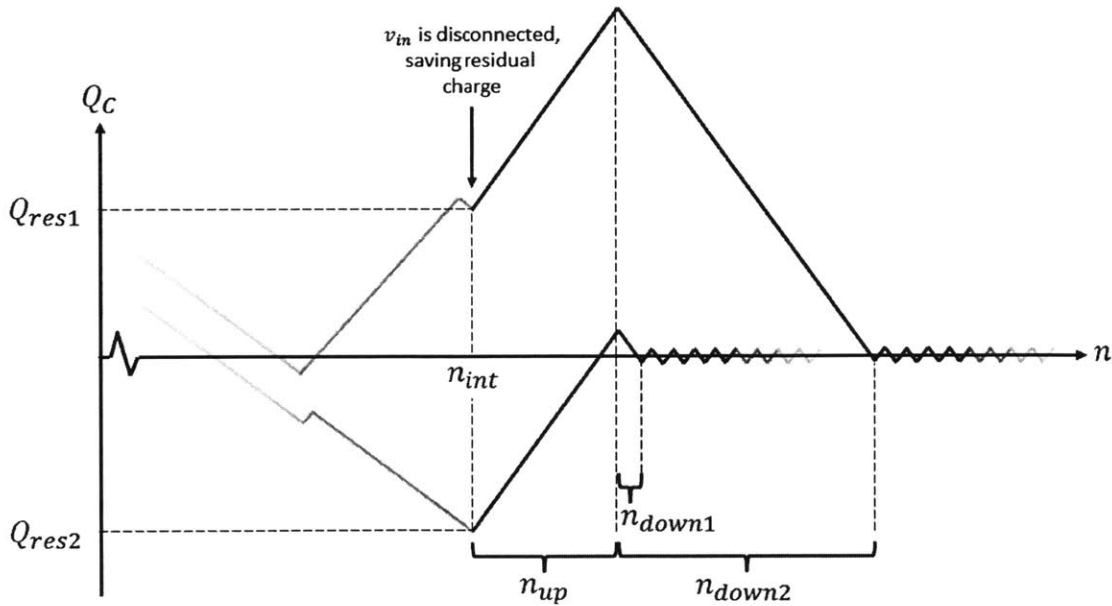


Figure 2-6: Landsburg ADC residual charge measurement

The up-integration is always performed before the down-integration to ensure that the output is always measured on the up-to-down comparator transition. This eliminates the effects of comparator hysteresis. This up-integration must be performed long enough to be certain that v_{int} is above the comparator threshold before the

down-integration. Since the residual charge, Q_{res} on the integrating capacitor is in the range of -14 to $+14$ clock cycles of charge, it can be assumed that v_{int} will be above the comparator threshold if you up-integrate for more than 14 clock cycles. In other words, it is necessary for n_{up} to be greater than 14. Similarly, $n_{down,max}$ must be greater than $(n_{up} + 14)$ clock cycles to ensure that the up-to-down comparator transition occurs.

The Landsburg ADC can be thought of as a split ADC. During the 'Measure State', it acts as a first-order CT $\Sigma\Delta$ ADC with a fixed number of switch transitions in order to find $\lfloor d_{out}/14 \rfloor$. It then proceeds to the 'Residue State', where it behaves like a dual-slope ADC to measure the remaining $d_{out} \bmod 14$. One part of the system remains to be explained: the autozero mechanism.

2.2.3 The Autozero Mechanism

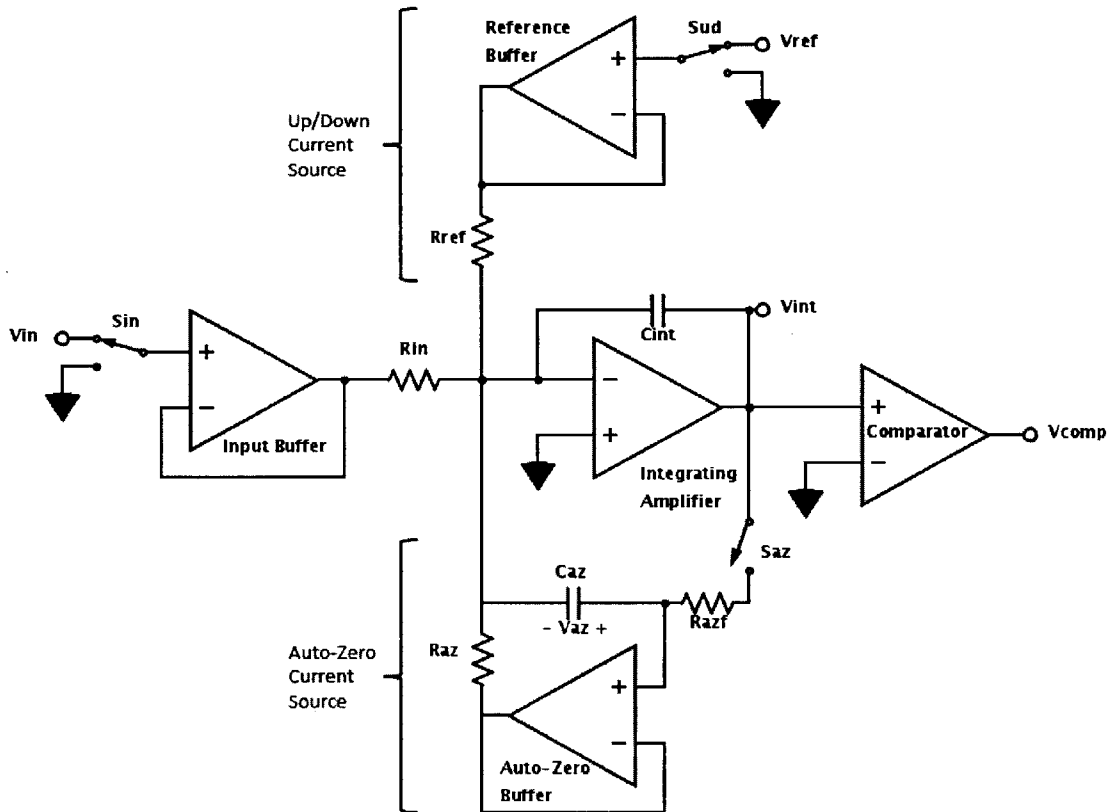


Figure 2-7: Landsburg ADC block diagram

Figure 2-7 shows a block diagram of the Landsburg ADC. As in Figure 2-3, R_{in} supplies the $\frac{V_{in}}{R_{in}}$ current which is integrated over $n_{integration} = 16N_{integration}$ clock cycles. In order to add or subtract the $\frac{V_{ref}}{2R_{ref}}$ current, the up-down switch (S_{ud}) is controlled to source a current of either 0 or $\frac{V_{ref}}{R_{ref}}$ through R_{ref} . The current through R_{az} is calibrated (by controlling the stored voltage on C_{az}) such that the combined current into the integrating capacitor is $\frac{V_{in}}{R_{in}} \pm \frac{V_{ref}}{2R_{ref}}$. This R_{az} current is nominally $-\frac{V_{ref}}{2R_{ref}}$, but will adjust to provide additional current to null the effects of the main offset sources in the circuit. These sources are as follows:

1. Integrating amplifier input offset voltage, $v_{offset,intamp}$
2. Integrating amplifier input bias current, $i_{bias,intamp}$
3. Input buffer input offset voltage, $v_{offset,inamp}$
4. Auto-zero buffer input offset voltage, $v_{offset,AZamp}$
5. Reference buffer input offset voltage, $v_{offset,refamp}$
6. Asymmetrical charge injection from up-down and down-up switching transitions
7. Comparator input offset voltage, $v_{offset,comp}$

The first six offset sources cause additional currents to flow into C_{int} . Sources 1-5 contribute additional currents of $\frac{v_{offset,intamp}}{R_{in}||R_{ref}||R_{az}}$, $i_{bias,intamp}$, $\frac{v_{offset,inamp}}{R_{in}}$, $\frac{v_{offset,AZamp}}{R_{az}}$ and $\frac{v_{offset,refamp}}{R_{ref}}$ respectively. The current from Source 6 is highly variable with switching speeds and temperature. The first auto-zero mechanism (AZ1) uses a feedback loop to store a precise voltage on C_{az} such that the current into C_{int} is $\frac{V_{in}}{R_{in}} \pm \frac{V_{ref}}{2R_{ref}}$. The second auto-zero mechanism (AZ2) ensures that C_{int} is charged to the comparator's transition voltage at the beginning of each measurement. This is essential as the comparator's transition voltage is $v_{offset,comp}$ above ground.

Figure 2-8 shows the ADC configuration during AZ1. Switches S_{in} and S_{ud} are both set to simulate the conditions of a zero input voltage: S_{in} grounds the input, and S_{ud} alternates between V_{ref} and ground every 8 clock cycles. This creates a sequence which repeats every 16 clock cycles, containing one down-to-up transition and one up-to-down transition. As with a zero input signal, this waveform spends equal time integrating up as it does integrating down. S_{az} is closed to form a feedback loop

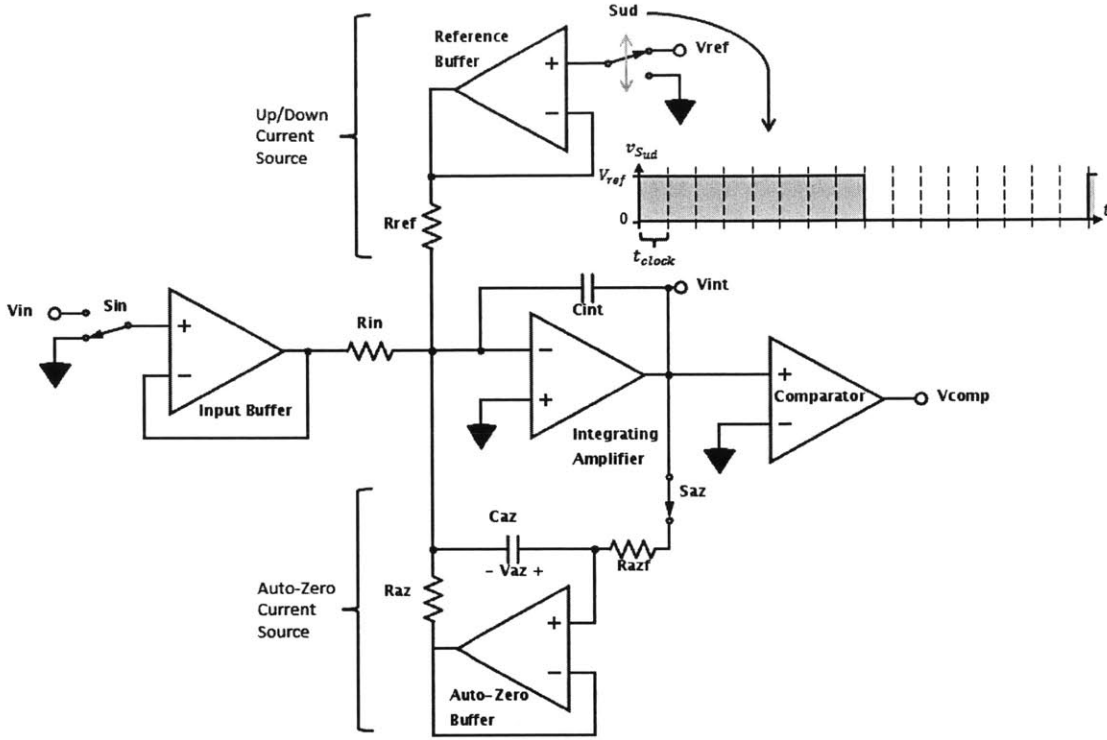


Figure 2-8: Landsburg ADC when performing AZ1

which serves the integration current (i.e. the current into C_{int}) to $\frac{V_{in}}{R_{in}} \pm \frac{V_{ref}}{2R_{ref}}$. With the grounded input buffer, the integration current should be $\pm \frac{V_{ref}}{2R_{ref}}$.

Consider the case where $v_{az} = 0$. With the switching waveform in Figure 2-5, the integration current will be 0 or $\frac{V_{ref}}{R_{ref}}$ (in other words, $\frac{V_{ref}}{2R_{ref}} \pm \frac{V_{ref}}{2R_{ref}}$) as well as the currents caused by offset sources 1-5. The feedback loop thus has to set v_{az} such that $i_{R_{az}} = -\frac{V_{ref}}{2R_{ref}}$ in addition to the currents from the offset sources. The resultant integrating current is the desired $\pm \frac{V_{ref}}{2R_{ref}}$.

The feedback loop dynamics are illustrated in Figure 2-9. There is a 2nd-order low-pass filter response from the switching voltage, $v_{S_{ud}}$ to the voltage stored on the auto-zero capacitor, v_{az} . This can be seen in the transfer function:

$$\frac{v_{az}(s)}{v_{S_{ud}}(s)} = -\frac{R_{az}}{R_{ref}} \left(\frac{1}{1 + sR_{az}C_{az} + sR_{az}C_{int}(1 + sR_{azf}C_{az})} \right)$$

$v_{S_{ud}}$ is a square wave between 0 and v_{ref} , of frequency $\frac{1}{16t_{clock}}$ with a 50% duty cycle. It is the superposition of a high-frequency, $\pm \frac{1}{2}v_{ref}$ square wave and an average voltage of

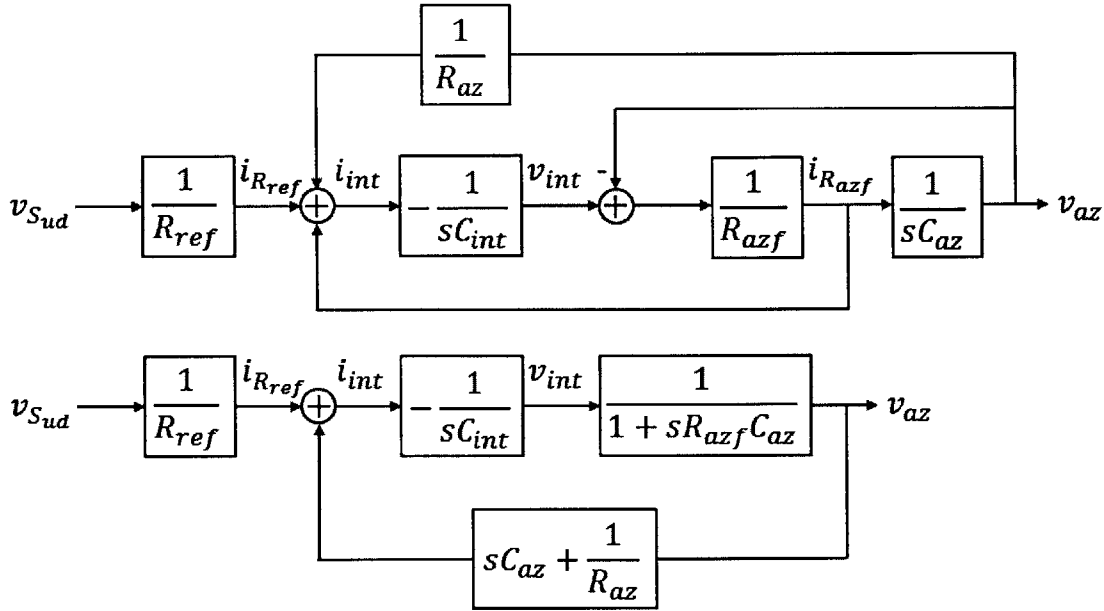


Figure 2-9: Block diagram of AZ1 feedback loop, complete (upper) and simplified (lower)

$\frac{1}{2}v_{ref}$. The low-pass filter response filters out the high-frequency switching, allowing the average voltage to be captured on the auto-zero capacitor. While the low loop bandwidth is necessary to filter out the high-frequency switching, it mandates that AZ1 must be run for a long period of time for v_{az} to converge to the full resolution of the ADC. A timing technique is used to further reject the high-frequency switching: due to the 2nd-order low-pass filtering, high frequencies will have a known phase-shift of 180° . Hence the opening of S_{az} (to sample & store v_{az} onto C_{az}) can be timed to the exact moment when the ripple is at its midpoint, to minimize the amount of ripple which is sampled. This is shown in Figure 2-10.

To show that this feedback loop causes the integrating current to converge to $\pm \frac{V_{ref}}{2R_{ref}}$, consider the circuit in Figure 2-8. During AZ1, the integrating current is the sum of currents from the up/down current source, the auto-zero current source and offset sources 1-5. Any low-frequency component of the integrating current will not be filtered out by the low-pass nature of the feedback loop, and will cause a shift in v_{az} . As a result, the loop will servo v_{az} until there is no longer any low-frequency component in the integrating current, converging to just the high-frequency $\pm \frac{V_{ref}}{2R_{ref}}$

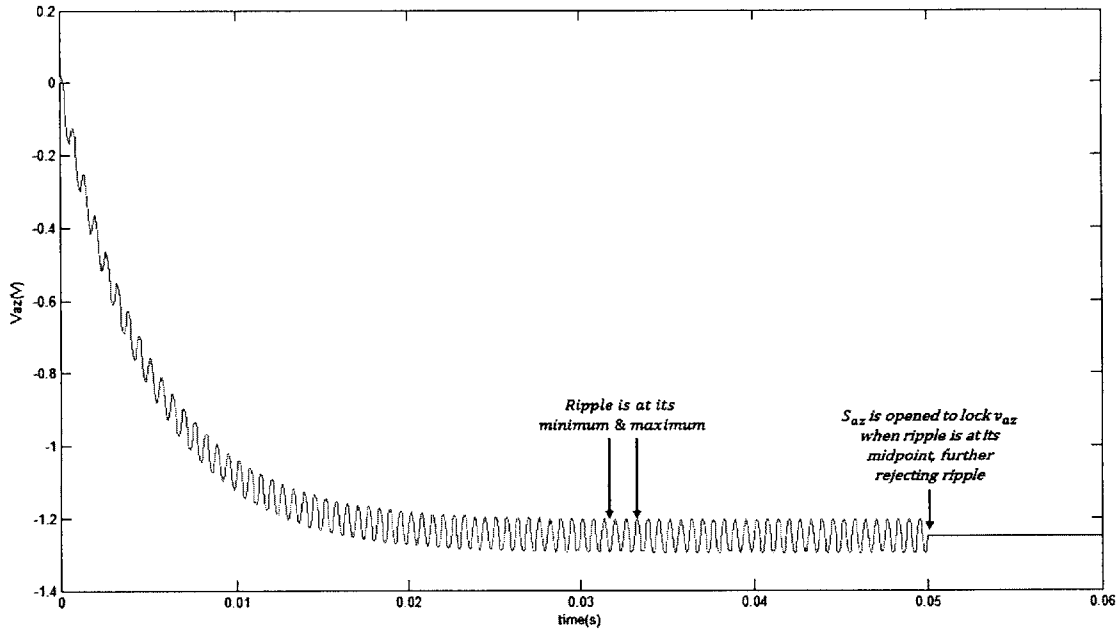


Figure 2-10: Ripple-rejection sampling of v_{az}

square wave. During the Measure State, S_{az} is opened and S_{in} is connected to v_{in} . This results in the integrating current becoming $\frac{v_{in}}{R_{in}} \pm \frac{V_{ref}}{2R_{ref}}$, controlled by the position of S_{ud} .

It is necessary for this feedback loop to have low bandwidth in order to filter out the high-frequency switching. As a result, it takes a long time (50ms in the original design) for the loop to converge to the full resolution of the ADC.

The purpose of the second auto-zero mechanism, AZ2, is to compensate for the comparator's input offset voltage (offset source 6). As the comparator's transition voltage is the baseline for 'zero' charge stored on the integration capacitor, it is necessary to set v_{int} to the comparator's transition voltage at the beginning of conversion. This is done with the circuit configured as in Figure 2-11. Due to the adjustment of v_{az} in AZ1, the integration current is either $\frac{V_{ref}}{2R_{ref}}$ or $-\frac{V_{ref}}{2R_{ref}}$, depending on the position of S_{ud} . To move v_{int} to the comparator's transition voltage, S_{ud} is set to integrate down if v_{comp} is high, and integrate up if v_{comp} is low. This creates the 'converge and dither' pattern for v_{int} which can be seen in Figure 2-11. As long as AZ2 is run long enough for v_{int} to travel from the supply rails to the comparator transition voltage

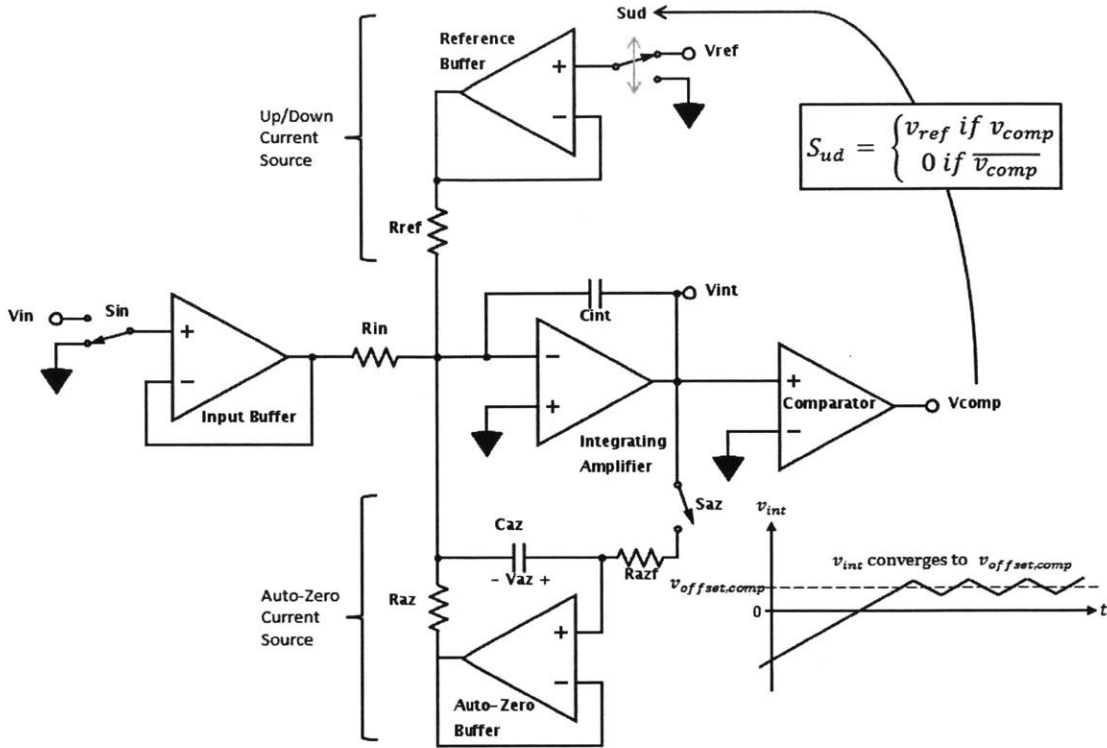


Figure 2-11: Landsburg ADC when performing AZ2

($v_{offset,comp}$), v_{int} will end up dithering around the $v_{offset,comp}$ by the end of AZ2. A change in polarity at the comparator's input will effect a change in integration current between $-\frac{V_{ref}}{2R_{ref}}$ and $\frac{V_{ref}}{2R_{ref}}$, and the time delay of this change, $t_{delay,AZ2loop}$ affects the closeness with which $v_{offset,comp}$ dithers around v_{int} . Neglecting noise, the following upper bound can be placed upon this dithering:

$$|v_{offset,comp} - v_{int}|_{dither} < \frac{V_{ref} t_{delay,AZ2loop}}{2R_{ref} C_{int}}$$

2.2.4 Putting It All Together

A single conversion using the Landsburg ADC thus involves the following sequential steps:

1. AZ1, to set v_{az} and cancel out offset sources 1-5.
2. AZ2, to set v_{int} to the comparator threshold and cancel out offset source 6.

3. Measure State, to measure the output down to a 14 LSB resolution. (Chapter 2.2.1)
4. Residue State, to measure the mod 14 residue of the output and provide unit clock resolution. (Chapter 2.2.2)

In the original Landsburg ADC described in [8], AZ1 was run for 50ms per conversion, whereas the Measure State was run for 100ms to reject 50Hz and 60Hz noise. AZ2 and the Residue State required a negligible duration of time. This gave the ADC a sample rate of roughly 6.6 Samples/s at 12-bit resolution with a 30kHz clock.

Chapter 3

System Design of the Modified Landsburg ADC

This chapter describes various architectural changes made to the Landsburg ADC to meet modern standards of ADC performance. Each change moves the design towards being a fully-monolithic, high-resolution, single-supply ADC with pseudo-differential inputs, implemented on a $.25\mu\text{m}$ CMOS process. The target specifications of this design are in Table 3.1.

Table 3.1: Target specifications for modified Landsburg ADC

Sample Rate	5 Samples/s
Resolution	19 bits
Power Consumption	approximately 1.5mW
Supply Voltage	3V - 5V
Reference Voltage	1.25V @ 3V supply, 2.5V @ 5V supply
Input Offset	<1 LSB
Gain Error	<0.01% over temp
INL	<1 LSB (<0.0002%) Full-Scale
Operating Temperature	-40°C - 125°C

3.1 Smaller Capacitors, Higher Resolution

The original Landsburg architecture has two large capacitors: the integrating capacitor and auto-zero capacitor, each of which are on the order of dozens of nanofarads [9]. These capacitors must be shrunk to a few hundred picofarads at most, so that they can be placed on-die. Consider the voltage change at the output of the integrator as it integrates a constant current, I , for one clock cycle (the integrator has negative gain):

$$\Delta v_{int} = -\frac{I}{C_{int}}t_{clock}$$

Reducing the capacitor size magnifies the voltage change. This is analogous to scaling up the entire v_{int} waveform, which will clip (causing a loss of linearity) as it is limited by the supply voltage rails. In order to reduce the capacitance while staying within the limits of the power supply, our options are to reduce the current and the length of each clock cycle (i.e. increase the clock frequency). There are other reasons for increasing the clock frequency. As the Landsburg ADC is an oversampling converter, its resolution increases linearly with clock frequency, so increasing clock frequency while keeping the Measure State time constant will increase the resolution of the converter.

3.1.1 Upper Limits on Resolution & Clock Frequency

What factors limit the clock frequency? Observe the main blocks of the Landsburg ADC in Figure 2-7. Of these, the input buffer and auto-zero buffer are only required to pass low-frequency signals. While the comparator's output must settle in less than one clock cycle, a fast-settling, low-power comparator can be built using a regenerative latching topology. The comparator's settling time is not the limiting factor on clock frequency.

In general, the most demanding and power-hungry parts of a system are those which require both high bandwidth and high precision. In the Landsburg ADC, these parts are the integrating amplifier and reference buffer. Consider the 16-clock return-to-zero sequences described in Chapter 2.2.1 and reproduced in the upper half

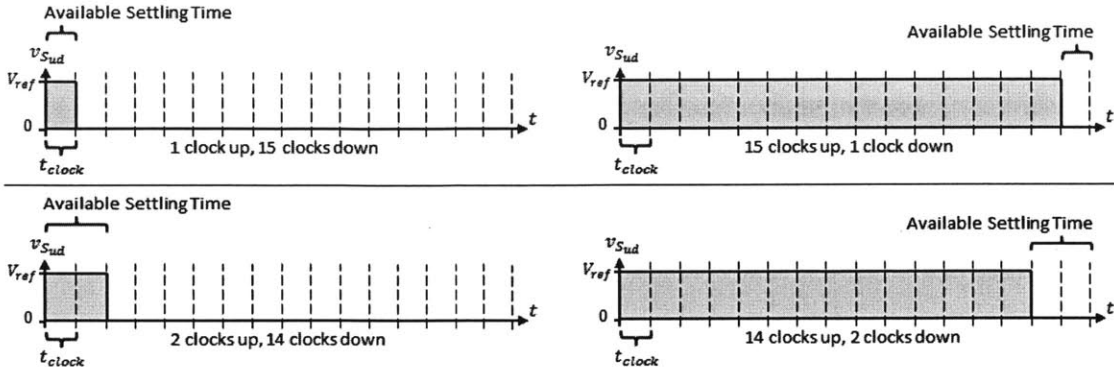


Figure 3-1: Landsburg ADC 16-clock switching sequences: original (upper) & modified (lower)

of Figure 3-1. The fastest transition which must be captured to full 19-bit accuracy is the single high pulse in the low-sequence and the single low pulse in the high-sequence. In other words, it is necessary for the integrating amplifier and reference buffer to achieve >19 -bit settling within a single clock cycle. The main constraint on the maximum clock frequency (and maximum resolution) of the Landsburg ADC is the full-resolution settling time of these two components.

Fast, high-resolution settling requires the use of a high-bandwidth, high-gain, dominant-pole amplifier. The limits of the manufacturing process will determine the maximum achievable performance of this amplifier, which in turn defines the maximum performance of the ADC. What can be done to extend the ADC's resolution beyond this limit?

Consider the alternative set of 16-clock return-to-zero sequences in the lower half of Figure 3-1. In the original set of sequences, every 16-clock sequence adds or subtracts 14 cycles of charge, as the first high pulse always negates the last low pulse. In this new set, every 16-clock sequence adds or subtracts 12 cycles of charge, as the first two high pulses always negate the last two low pulses. As described in Chapter 2.2.2, the original Landsburg ADC's Measure State measures $\lfloor d_{out}/14 \rfloor$ and its Residue State measures $d_{out} \bmod 14$. In this modified version, the Measure State measures $\lfloor d_{out}/12 \rfloor$ and the Residue State measures $d_{out} \bmod 12$. The overall gain

equation is now:

$$v_{in} = v_{ref} \frac{R_{in}}{2R_{ref}} \left(\frac{12(2N_{low} - N_{integration}) + n_{down} - n_{up}}{16N_{integration}} \right)$$

As each 16-clock sequence now causes a change of 12 (instead of 14) cycles of charge, we would need a clock which is $\frac{14}{12} = 116.7\%$ the speed of an equal-resolution original Landsburg ADC. However, the integrating amplifier and reference buffer now have 2 clock cycles to achieve >19-bit settling, and a correspondingly lower bandwidth. While the required clock speed has increased by 16.7%, the required bandwidth for these two circuit blocks has gone down to $\frac{1}{2} \frac{14}{12} = 58.3\%$ of its original value. For a given amplifier settling time, the ADC can now be run to a clock speed and resolution which is $2 \frac{12}{14} = 171.4\%$ of its original limit.

We can generalize by saying that the return-to-zero sequences are m cycles long. Within each m -clock sequence, the first n cycles are always high and the last n cycles are always low. The original Landsburg then used $m = 16$ and $n = 1$, whereas the modified Landsburg uses $m = 16$ and $n = 2$. In an ADC with R -bit resolution, the integrating amplifier and reference buffer are required to settle to over R -bit accuracy within nt_{clock} time. Every m -clock sequence adds or subtracts $(m - 2n)$ cycles of charge. The range of possible outputs is 2^{R-1} counts above and below ground, requiring the Measure State to run for $(2^{R-1} \frac{m}{m-2n})$ clocks. The generalized gain equation is then:

$$v_{in} = v_{ref} \frac{R_{in}}{2R_{ref}} \left(\frac{(m - 2n)(2N_{low} - N_{integration}) + n_{down} - n_{up}}{mN_{integration}} \right)$$

3.1.2 A Discussion of m and n

In order to optimize our choice of m and n , we must consider their effect on the output swing of the integrating amplifier. As previously established, it is essential that its output does not clip in order to preserve linearity. Every m clock cycles, S_{ud} is set such that v_{int} moves towards the comparator threshold ($v_{offset,comp}$) during the following m clock cycles. The largest possible voltage difference between v_{int} and $v_{offset,comp}$ is

the furthest distance that v_{int} can travel away from $v_{offset,comp}$ during those m clock cycles. The upper and lower bounds on this voltage difference correspond to the minimum and maximum input current (i_{in}), beyond which the ADC goes underrange or overrange.

What is the minimum and maximum input current? After AZ1 calibration, we know the integration current, $i_{int} = \frac{V_{in}}{R_{in}} \pm \frac{V_{ref}}{2R_{ref}} = i_{in} + i_{ud}$, where i_{ud} is the up/down current. If the input current is within bounds, this means that the average up/down current is of sufficient magnitude to overwhelm the input current and pull v_{int} towards the comparator threshold. The most extreme average up/down currents are achieved if S_{ud} performs just the 'high' sequence ($(m-n)$ high pulses followed by n low pulses) or just the 'low' sequence (n high pulses followed by $(m-n)$ low pulses) for the entire duration of the Measure State. Thus the two most extreme average up/down currents are $\frac{V_{ref}}{2R_{ref}} \frac{m-2n}{m}$ and $-\frac{V_{ref}}{2R_{ref}} \frac{m-2n}{m}$. It follows that the minimum and maximum input currents are just within $-\frac{V_{ref}}{2R_{ref}} \frac{m-2n}{m}$ and $\frac{V_{ref}}{2R_{ref}} \frac{m-2n}{m}$.

Now we can finally calculate the maximum and minimum voltage difference between v_{int} and $v_{offset,comp}$. As the integrator has negative gain, the maximum difference is when $i_{in} = -\frac{V_{ref}}{2R_{ref}} \frac{m-2n}{m}$ and S_{ud} performs the 'low' sequence. v_{int} starts just below $v_{offset,comp}$, travels downwards for n cycles (integrating a current of $-\frac{V_{ref}}{2R_{ref}} \frac{m-2n}{m} + \frac{V_{ref}}{2R_{ref}}$) and then travels upwards for $(m-n)$ clock cycles (integrating a current of $-\frac{V_{ref}}{2R_{ref}} \frac{m-2n}{m} - \frac{V_{ref}}{2R_{ref}}$). Calculating $[v_{int} - v_{offset,comp}]_{max}$:

$$[v_{int} - v_{offset,comp}]_{max} = -\frac{t_{clock}}{C_{int}} \frac{v_{ref}}{2R_{ref}} \left(n \left(-\frac{m-2n}{m} + 1 \right) + (m-n) \left(-\frac{m-2n}{m} - 1 \right) \right)$$

$$[v_{int} - v_{offset,comp}]_{max} = \frac{t_{clock}}{C_{int}} \frac{v_{ref}}{2R_{ref}} 2(m-2n)$$

Similarly, the minimum difference is when $i_{in} = \frac{V_{ref}}{2R_{ref}} \frac{m-2n}{m}$ and S_{ud} performs the 'high' sequence. v_{int} starts just above $v_{offset,comp}$, travels downwards for $(m-n)$ cycles (integrating a current of $\frac{V_{ref}}{2R_{ref}} \frac{m-2n}{m} + \frac{V_{ref}}{2R_{ref}}$) and then travels upwards for n clock cycles (integrating a current of $\frac{V_{ref}}{2R_{ref}} \frac{m-2n}{m} - \frac{V_{ref}}{2R_{ref}}$). The lowest voltage in this sequence is after $(m-n)$ cycles, just before v_{in} begins travelling upwards. Calculating

$[v_{int} - v_{offset,comp}]_{min}$:

$$[v_{int} - v_{offset,comp}]_{min} = -\frac{t_{clock}}{C_{int}} \frac{v_{ref}}{2R_{ref}} \left((m-n) \left(\frac{m-2n}{m} + 1 \right) \right)$$

$$[v_{int} - v_{offset,comp}]_{min} = -\frac{t_{clock}}{C_{int}} \frac{v_{ref}}{2R_{ref}} 2 \left(m - 2n + \frac{n^2}{m} \right)$$

It can be seen that the magnitude of $[v_{int} - v_{offset,comp}]_{min}$ is slightly greater than $[v_{int} - v_{offset,comp}]_{max}$. This asymmetry is because $v_{S_{ud}}$ in Figure 3-1 always goes high at the beginning of the sequence before going low, in other words, v_{int} starts moving downwards before moving upwards. This asymmetry can be reversed by switching the order of the m -clock sequences, by having the first n pulses always be low and the last n pulses always be high.

With all these equations, how do we choose m and n ? n can range from 1 to $\frac{m}{2}$. While increasing n loosens the settling-time requirements for the integrating amplifier and reference buffer, it also increases the number of clock cycles required to perform a conversion, as does decreasing m . As $2n$ approaches m , the number of clock cycles approaches infinity. One approach is to start with $n = 1$ and increase n if the amplifier settling times are just too slow for the target speed & resolution. Increasing m decreases the number of clock cycles per conversion (allowing the use of a slower clock) but also increases the required size of C_{int} to keep the integrator output swing from clipping. The eventual choice of $m = 16$ and $n = 2$ is a compromise between these effects.

3.1.3 Choosing C_{int} , Resolution & Clock Frequency

With $m = 16$, $n = 2$ and a total Measure State time of 0.1s (to reject 50Hz and 60Hz), we can calculate a need for at least $(2^{R-1} \frac{m}{m-2n}) \approx 350000$ clock cycles. With a target resolution of 19 bits, this implies a clock frequency of $>3.5\text{MHz}$; 3.6MHz was chosen for redundancy. $R_{ref} = 200k\Omega$ and $C_{int} = 50\text{pF}$ were also chosen. With a 2.5V reference, this results in a 0.84V to -0.85V integrator output swing around the comparator threshold. Using the smaller 1.25V reference, the range becomes 420mV

to -430mV . As described in Chapter 4.4, this fairly small voltage swing was chosen as it was not possible to build an integrating amplifier with rail-to-rail outputs which also met the gain, bandwidth and power requirements.

3.2 Single-Supply Operation & Eliminating the Reference Buffer

The original Landsburg design uses bipolar power supplies and a ground-referenced voltage reference. The switching voltage (controlled by S_{ud}) varies between 0 and v_{ref} relative to the integrator's summing node, which is biased at ground. During AZ1, the negative gain of the $v_{S_{ud}}$ to v_{az} transfer function causes v_{az} to servo to a voltage below the integrator's summing node.

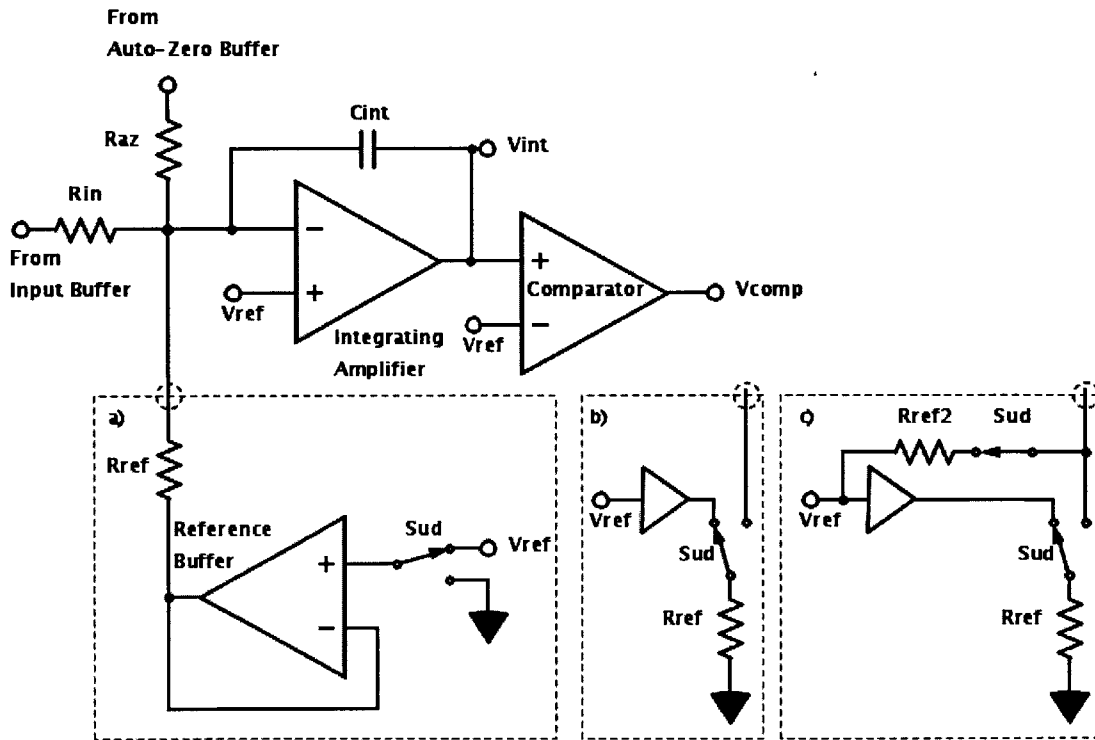


Figure 3-2: Landsburg ADC single supply modifications, with reference buffer (a), without reference buffer (b), with constant summing-node impedance (c)

In order to adapt the Landsburg to single-supply operation, it is necessary to flip it

upside-down. As shown in Figure 3-2a, the integrator summing node and comparator threshold are now biased at v_{ref} . As the amplifiers and comparator are powered from ground to the positive rail (v_{dd}), there is a voltage headroom of $-v_{ref}$ to $(v_{dd} - v_{ref})$ around the summing node. In this new configuration, the switching voltage now varies between $-v_{ref}$ and 0 relative to the integrator summing node. v_{az} then servos to a voltage above the integrator summing node.

In this new configuration, the summing node is now $(v_{ref} + v_{offset,intamp})$ above ground, where $v_{offset,intamp}$ is the input offset of the integrating amplifier. Assuming that $v_{offset,intamp}$ is small, R_{ref} can simply be connected between the summing node and ground to sink a $(\frac{v_{ref}}{R_{ref}} + \frac{v_{offset,intamp}}{R_{ref}})$ reference current. A switch in series with R_{ref} allows this current to be turned on and off, as shown in Figure 3-2b. A double-throw switch is used to connect R_{ref} to a basic V_{ref} buffer when the reference current is not being sunk from the summing node. This ensures that R_{ref} has consistent, code-independent self-heating, so that code-dependent temperature (and resistance) changes do not introduce non-linearity. The reference buffer is a fast-settling, high-gain, rail-to-rail amplifier. Its removal significantly reduces the cost of the Landsburg architecture.

In order to maintain consistent summing node impedance (and preserve linearity), an additional reference resistor (R_{ref2}) is added, as shown in Figure 3-2c. This resistor is connected from V_{ref} to the summing node when R_{ref} is not connected. As this resistor pulls very minimal current ($\frac{v_{offset,intamp}}{R_{ref2}}$), its matching to R_{ref} is not critical. In simulation, as much as 3% mismatch between R_{ref} and R_{ref2} did not produce a measurable increase in INL. This $\frac{v_{offset,intamp}}{R_{ref2}}$ current also cancels out the $\frac{v_{offset,intamp}}{R_{ref}}$ term of the R_{ref} reference current, removing the gain error caused by the integrating amplifier's input offset.

This description is incomplete because it assumes that there is no voltage drop across the switches. Taking switch resistance into account, the reference current through R_{ref} will be less than $\frac{v_{ref}}{R_{ref}}$ and no longer ratiometric with R_{in} , increasing the ADC's gain drift over temperature. The next section describes a method to compensate for finite, nonlinear switch resistance.

3.2.1 Switch Resistance Compensation

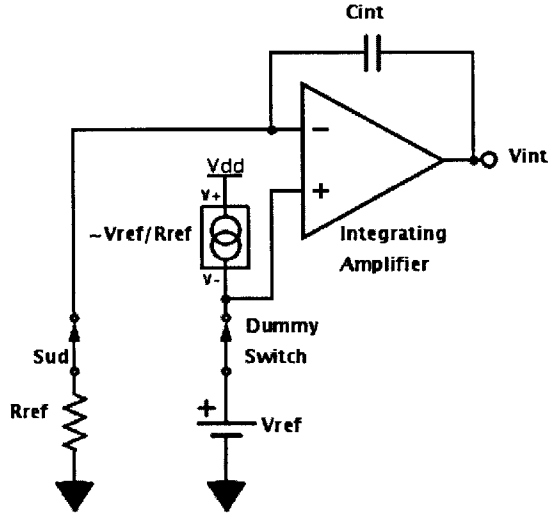


Figure 3-3: Simplified diagram of switch resistance compensation

As illustrated in Figure 3-3, switch resistance compensation is performed by using a dummy switch to replicated the voltage drop across S_{ud} . The intended current through R_{ref} is $\frac{v_{ref}}{R_{ref}}$, so a rough approximation of this current is made (using a resistor and current mirror, not shown) and sourced into the dummy switch. Denoting the voltage across the switch as v_{switch} , we can describe the voltage at the integrating amplifier's positive input:

$$v_{+,intamp} = v_{ref} + v_{switch,dummy}$$

Assuming the amplifier's inputs are at the same voltage:

$$v_{-,intamp} = v_{+,intamp} = v_{ref} + v_{switch,dummy}$$

$$v_{-,intamp} = i_{R_{ref}} R_{ref} + v_{switch,S_{ud}} = v_{ref} + v_{switch,dummy}$$

The dummy switch and S_{ud} are well-matched and in close thermal proximity. If they are carrying almost the same current, then $v_{switch,S_{ud}} \approx v_{switch,dummy}$. This implies that $i_{R_{ref}} R_{ref} \approx v_{ref}$, so $i_{R_{ref}} \approx \frac{v_{ref}}{R_{ref}}$ and the switches are carrying almost

the same current. Figure 3-5 shows a temperature sweep over 100 Monte Carlo simulations, comparing the current of the switch and resistor against just a resistor. With a 1.25V reference, the $\pm 3\sigma$ worst-case deviation from purely resistive behavior is 0.38ppm/ $^{\circ}\text{C}$, producing a gain error of 0.006% over the entire operating temperature. The corresponding worst-case deviation using a 2.5V reference is 0.25ppm/ $^{\circ}\text{C}$, or 0.004%. Both are within the $<0.01\%$ gain error target.

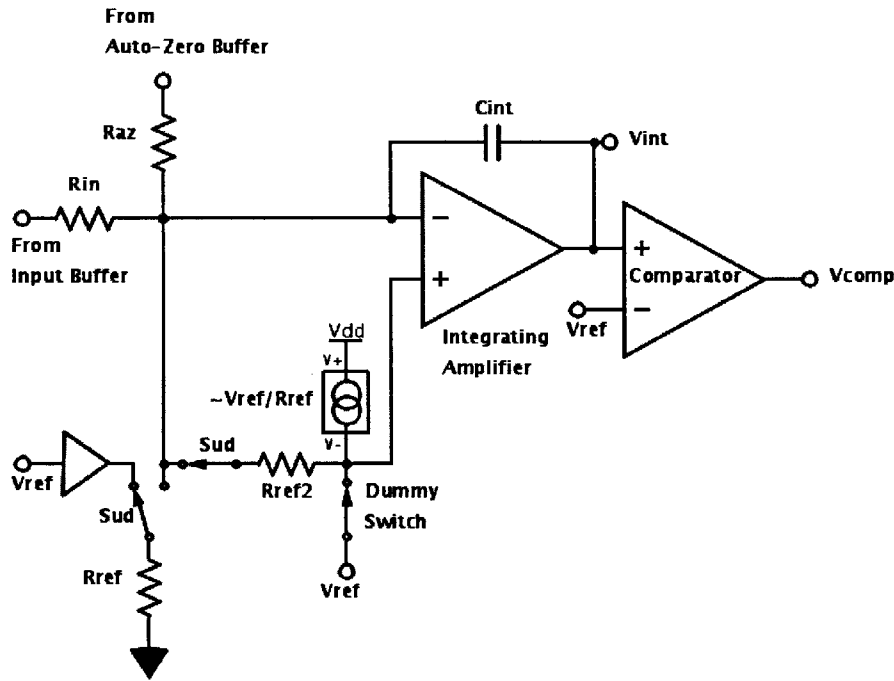


Figure 3-4: Implementation of switch resistance compensation

3.3 Pseudo-Differential Inputs & Auto-Zero

Consider the auto-zero mechanism illustrated in Figure 2-9. By using an up/down waveform with a 50% duty cycle during AZ1, we are instructing the ADC to regard the ground voltage at the input buffer (as set by S_{in}) as the zero-point of the measurement, and store this information as a voltage across C_{az} . If we switch S_{ud} between differential input pins v_{in+} and v_{in-} instead of v_{in} and ground, the ADC is able to

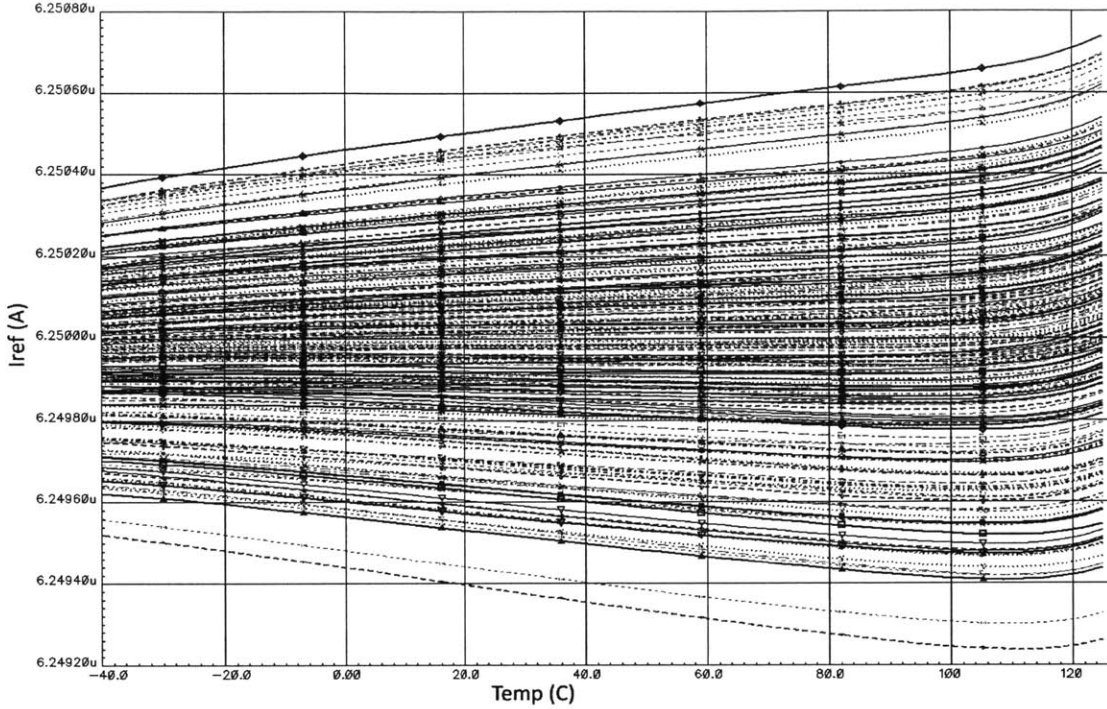


Figure 3-5: 100 Monte Carlo simulations of reference current drift over temperature, with $v_{ref} = 1.25V$

measure a pseudo-differential¹ voltage $v_{in} = (v_{in+} - v_{in-})$. In this configuration, AZ1 is essentially an analog Measure State which stores its measurement of v_{in-} using C_{az} as analog memory. The auto-zero mechanism is thus modified to provide pseudo-differential inputs. Figure 3-6 illustrates the input buffer connected in this manner, including the modifications from Chapter 3.2.

The next step is to replace R_{azf} with a gm-cell, as shown in Figure 3-7. This is done to relax the design requirements on the integrating amplifier, which already needs high gain and fast settling behavior. If the integrating amplifier directly drives R_{azf} , it will also need a low-impedance output stage and significant output swing. These two requirements go away if we replace R_{azf} with a MOS-input, rail-to-rail gm-cell. Figure 3-8 shows the updated AZ1 feedback loop dynamics. It can be shown that this loop is stable (with phase margin $> 45^\circ$) if $gm_{azf}R_{az}\frac{C_{az}}{C_{int}} > 1$.

¹In a fully differential system, v_{in+} and v_{in-} would be measured simultaneously. This ADC is ‘pseudo-differential’ because v_{in-} is measured during AZ1, followed by v_{in+} which is measured during the Measure State.

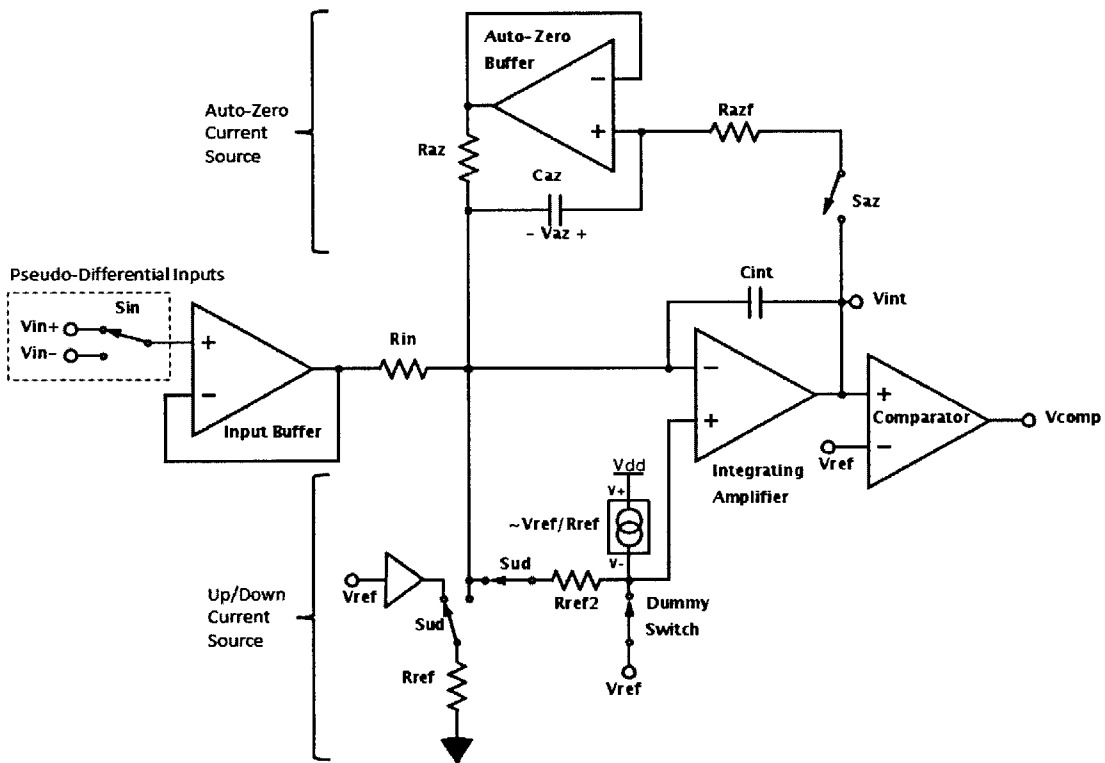


Figure 3-6: Landsburg ADC with pseudo-differential inputs & modified up/down current source

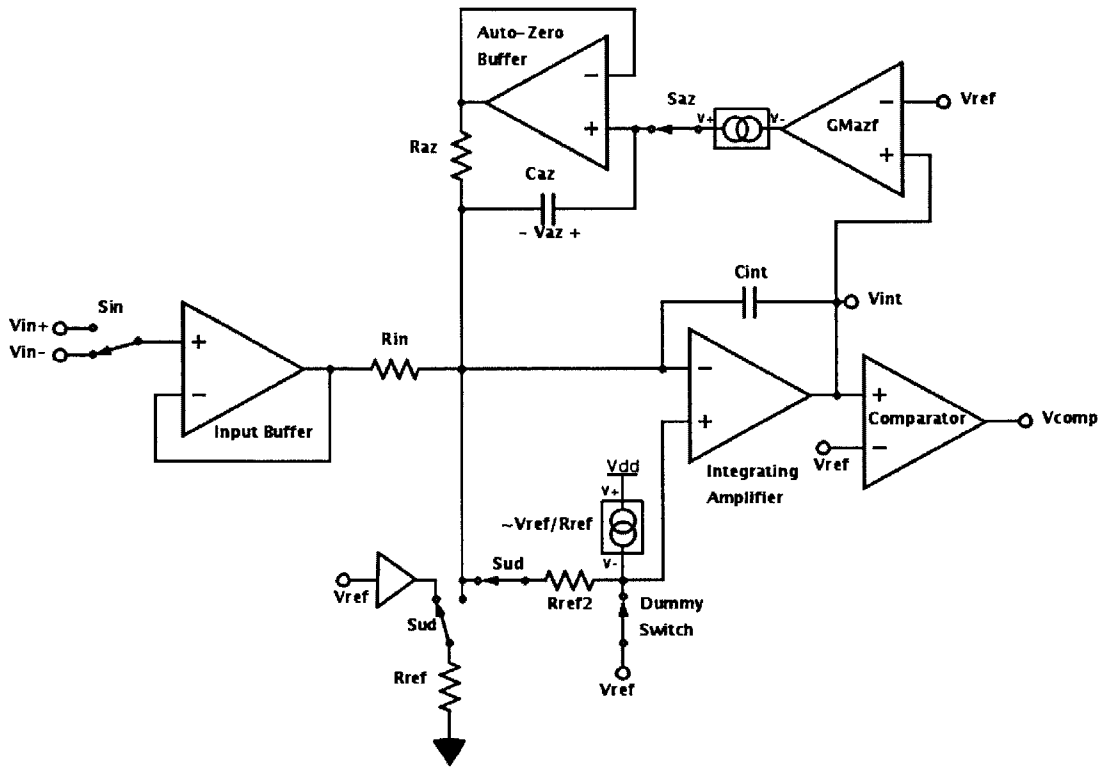


Figure 3-7: Landsburg ADC with gm-cell replacing R_{azf} , in AZ1 configuration

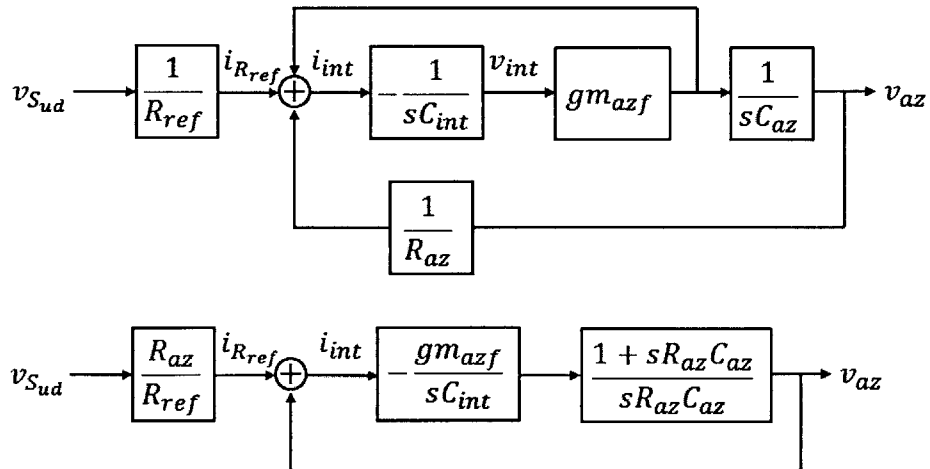


Figure 3-8: Block diagram of AZ1 feedback loop with gm-cell replacing R_{azf} , complete (upper) & simplified (lower)

How do we pick a value for R_{az} ? Denoting $v_{summingnode}$ as the voltage at the integrator summing node, the auto-zero current, i_{az} is:

$$i_{az} = \frac{v_{az} - v_{summingnode}}{R_{az}}$$

$$v_{summingnode} = v_{ref} + v_{dummyswitch} + v_{offset,comp} \approx v_{ref}$$

$$i_{az} \approx \frac{v_{az} - v_{ref}}{R_{az}}$$

The value of R_{az} is then chosen to set the range of auto-zero current, and hence the range of acceptable voltages for v_{in} . Values of $R_{az} \approx 200k\Omega$ can be expected for a 5V ADC input range.

3.3.1 Issues With Switch Leakage Current

One major hurdle in implementing the auto-zero mechanism on die is the leakage current of S_{az} during the Measure State. In order to reject 50Hz and 60Hz noise, the Measure State runs for 0.1 seconds, during which S_{az} is in the off position to prevent any change in voltage of C_{az} . The following calculation estimates the input offset (d_{offset} , in LSBs) resulting from a switch leakage current, i_{leak} . For an ADC with R -bit resolution and a Measure State duration of $t_{meas} = 0.1s$, we can calculate the difference in integrated charge caused by a 1 LSB change at the input voltage.

The full input current range, $|i_{in}| \leq \frac{v_{ref}}{2R_{ref}} \frac{m-2n}{m}$ represents an output code range of $\pm 2^{R-1}$ LSBs. Hence a single LSB of input current:

$$i_{in,1LSB} = \frac{1}{2^{R-1}} \frac{v_{ref}}{2R_{ref}} \frac{m-2n}{m}$$

Integrated over t_{meas} , this creates the following change in integrated charge:

$$Q_{int,1LSB} = \frac{1}{2^{R-1}} \frac{v_{ref} t_{meas}}{2R_{ref}} \frac{m-2n}{m}$$

$Q_{int,1LSB}$ is used to normalize the change in integrated charge caused by a non-zero

switch leakage current. Calculating the drift in C_{az} voltage, Δv_{az} :

$$\Delta v_{az} = \int \frac{i_{leak}}{C_{az}} dt$$

Charge loss due to switch leakage:

$$\Delta Q_{int,leak} = \int_0^{t_{meas}} \Delta i_{az} dt = \int_0^{t_{meas}} \frac{\Delta v_{az}}{R_{az}} dt = \int_0^{t_{meas}} \frac{i_{leak}}{R_{az} C_{az}} t dt = \frac{1}{2} \frac{i_{leak}}{R_{az} C_{az}} t_{meas}^2$$

Normalizing against $Q_{int,1LSB}$ to find the input offset (in LSBs) due to switch leakage:

$$d_{offset} = \frac{\Delta Q_{int,leak}}{Q_{int,1LSB}} = 2^{R-1} \frac{R_{ref}}{R_{az}} \frac{i_{leak} t_{meas}}{v_{ref} C_{az}} \frac{m}{m-2n}$$

If the largest C_{az} we are willing to fit on-die is about 200pF, we can estimate the resulting input offset using typical values of $R = 19$, $R_{ref} = 200k\Omega$, $R_{az} = 200k\Omega$, $t_{meas} = 0.1s$, $C_{az} = 200pF$, $v_{ref} = 1.25V$, $m = 16$ and $n = 2$. Then:

$$d_{offset} \approx 1.4 \times 10^{14} i_{leak}$$

This formula implies that to get the input offset below 0.5LSB, we would need a worst-case switch leakage current of under 3.6fA. A more realistic switch leakage current (while still difficult to achieve) is 200fA, which would result in 56 LSBs of offset. The following section proposes a method to achieve sub-LSB offset using a switch with a worst-case leakage of about 200fA.

3.3.2 Mixed-Signal Feedback Loop

Consider the equation from the previous section:

$$d_{offset} = \frac{\Delta Q_{int,leak}}{Q_{int,1LSB}} = 2^{R-1} \frac{R_{ref}}{R_{az}} \frac{i_{leak} t_{meas}}{v_{ref} C_{az}} \frac{m}{m-2n} \approx \frac{5.6 \times 10^6}{R_{az}}$$

A value of $R_{az} = 13M\Omega$ can be used to bring the offset below 0.5LSB, but this brings up two practical problems.

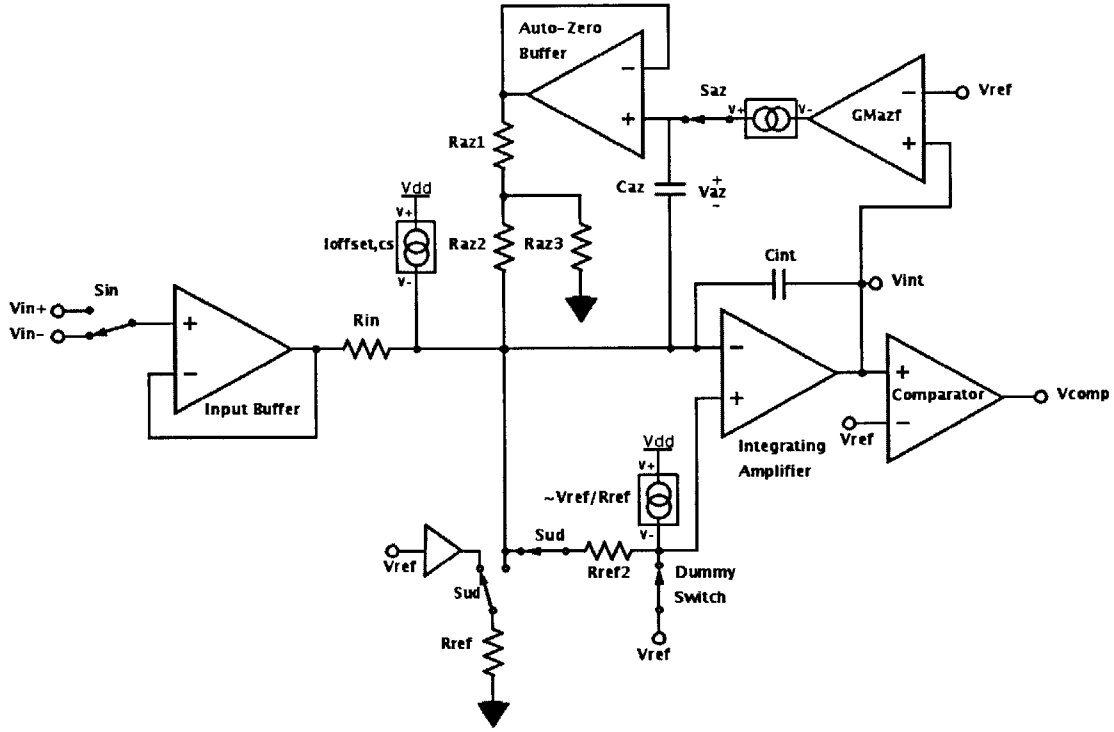


Figure 3-9: Landsburg ADC with current-splitting auto-zero resistors

The first problem is that $13M\Omega$ is a very large resistor to implement on-chip. Figure 3-9 shows a current-splitting method to synthesize this large resistor from three smaller resistors, R_{az1} , R_{az2} and R_{az3} . This generates an equivalent resistance of $R_{az,equiv} = (R_{az1} + R_{az2} || R_{az3}) \frac{R_{az2} + R_{az3}}{R_{az3}}$. In order to obtain the desired $R_{az,equiv} = 13M\Omega$, $R_{az1} = R_{az2} = 600k\Omega$ and $R_{az3} = 30k\Omega$ can be used. This current-splitting technique also introduces an offset of $i_{offset,cs} \approx \frac{v_{ref}}{R_{az3} + R_{az1} || R_{az2}} \frac{R_{az1}}{R_{az1} + R_{az2}}$, which must be compensated for with an additional $i_{offset,cs}$ current source into the summing node.

The second problem is that a large R_{az} , constrained by the limits of the power supply, can only provide a limited range of auto-zero current. This corresponds to a limited range of acceptable voltages for v_{in-} . This is sufficient if we are performing single-ended measurements, such that v_{in-} will always be at a known voltage. For example, if v_{in-} is always at v_{ref} , then the center of the auto-zero current range can be shifted to v_{ref} with an additional $\frac{v_{ref}}{2R_{ref}}$ current source into the summing node. Then R_{az} will only need enough auto-zero current range to compensate for the various offset

sources discussed in Chapter 2.2.3.

But what if we want to achieve full pseudo-differential behavior, where v_{in-} can be anywhere in the full voltage range? One possibility is shown in Figure 3-10: a low-resolution current DAC (with an output current range of $\frac{v_{ref}}{R_{ref}}$ to 0) can be used to provide most of the auto-zero current while R_{az} (the ‘analog auto-zero’) provides the residue current, filling in the spaces between the bits of the DAC. This arrangement couples the sub-LSB precision of the analog auto-zero with the stability and range of the DAC. This then turns into a controls problem - how can the DAC be controlled in such a way that the loop is stable, and the sum of DAC and analog auto zero currents converges to the correct value?

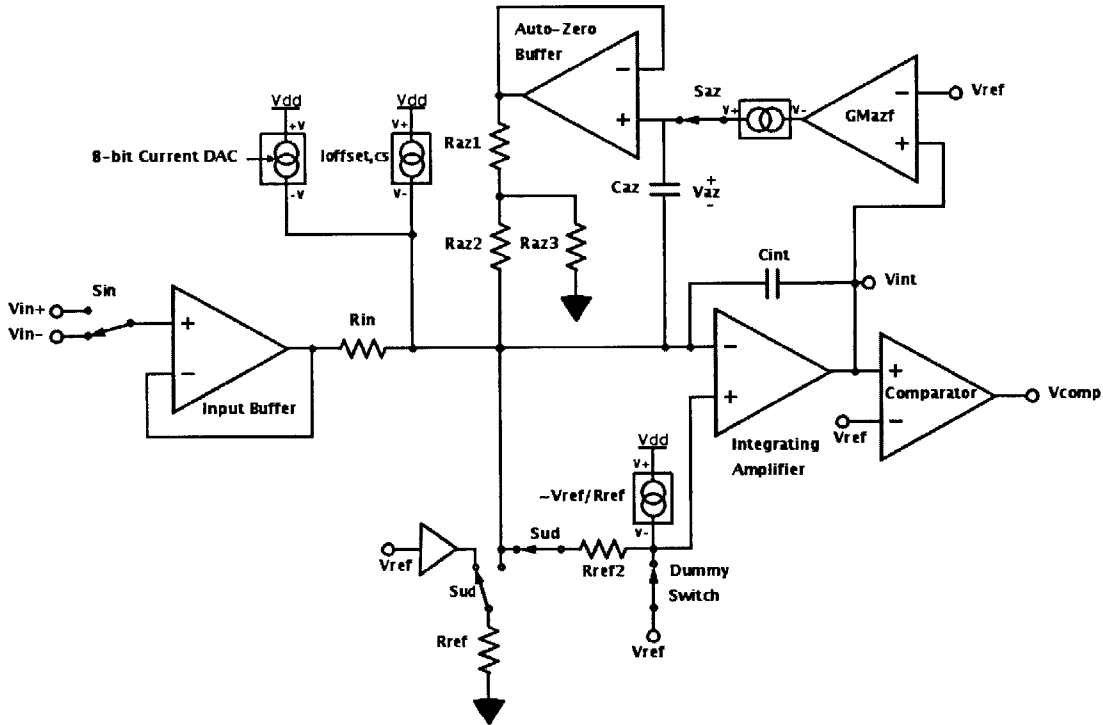


Figure 3-10: Landsburg ADC with 8-bit auto-zero current DAC

While many different methods were tried, this thesis will only discuss the most promising approach. The analog auto-zero is simply allowed to run as usual, with values $v_{ref,equiv} = 13M\Omega$, $gm_{azf} = \frac{1}{54k\Omega}$ and $C_{az} = 200pF$. At the same time, every 8 clock cycles, the DAC output is adjusted based on the comparator output. If v_{comp} is

low, the DAC current is decremented, so that v_{int} tends to increase. If v_{comp} is high, the DAC current is incremented, so that v_{int} tends to decrease. The convergence of DAC input code is shown for various v_{in-} voltages in Figure 3-11. Once the DAC 8-bit input code has converged to within an LSB of the required current, it dithers back and forth across that last LSB. 40ms after the start of the AZ1 process, its input code is locked to halt the dithering. This allows the analog auto-zero to converge to its final value. While $gm_{azf} = \frac{1}{54k\Omega}$ is the minimum transconductance necessary to stabilize the DAC feedback loop, it is too much to provide adequate filtering of the high-frequency switching. As a workaround, after the DAC code is locked, gm_{azf} is reduced to $\frac{1}{108k\Omega}$.

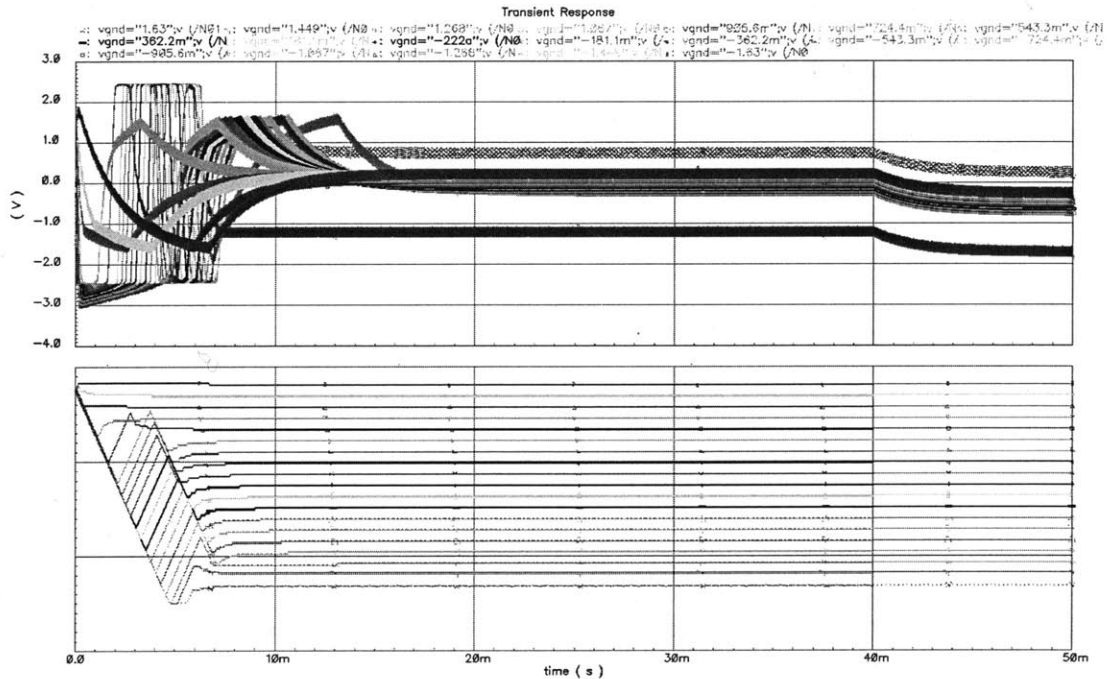


Figure 3-11: Transient simulation of mixed-signal AZ1 for various values of v_{in-} : v_{az} (upper) & DAC input code (lower)

It is interesting to note that the DAC feedback loop is not stable unless the analog auto-zero runs at the same time. To understand this, we will need a way to analyze the non-linear relationship between the voltage at the input of the comparator (v_{int}) and the resulting change in output current of the DAC (Δi_{dac}). An approximate analysis will be made using describing functions [11].

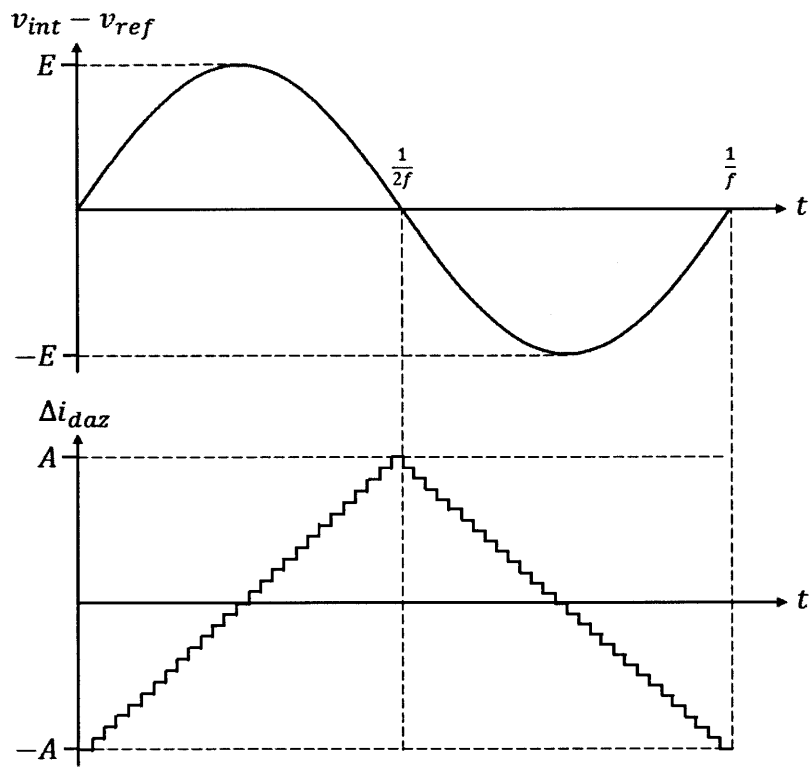


Figure 3-12: Change in DAC current, Δi_{dac} , due to a sine-wave at comparator input

Consider a sine wave at the input of the comparator, centred around v_{ref} , of frequency f and amplitude E . Figure 3-12 shows that during the sine wave's first half-cycle (of duration $\frac{1}{2f}$), the comparator output will be high, and the DAC current will decrement every 8 clock cycles. During the sine wave's second half-cycle (of equal duration), the comparator output will be low, and the DAC current will increment every 8 clock cycles. This causes Δi_{dac} to take the shape of a stepped triangle wave, phase-shifted -90° from the input, with amplitude A . Each current DAC bit represents a change in current of $\frac{1}{2^8} \frac{v_{ref}}{R_{ref}}$ and $\frac{1}{8t_{clock}} \frac{1}{2f}$ steps will occur during the first half-cycle. Hence:

$$A = \frac{v_{ref}}{2 \cdot 2^8 \cdot 16t_{clock} f R_{ref}}$$

A triangle wave of amplitude A contains a first-harmonic of magnitude $\frac{8A}{\pi^2}$, so the approximate $\frac{i_{dac}(s)}{v_{int}(s)}$ transfer function is:

$$\frac{i_{dac}(s)}{v_{int}(s)} = \frac{1}{j} \frac{8A}{\pi^2 E} = \frac{v_{ref}}{2^{10} \pi^2 E t_{clock} R_{ref}} \frac{1}{j f} = \frac{v_{ref}}{2^9 \pi E t_{clock} R_{ref}} \frac{1}{s} = \frac{G_{df}}{E} \frac{1}{s}$$

where $s = j\omega$ and $G_{df} = \frac{v_{ref}}{2^9 \pi t_{clock} R_{ref}}$. In other words, the v_{int} to i_{dac} transfer function can be approximated as an integrator with a gain inversely proportional to the input amplitude, E . We can now model the dynamics of the joint feedback loops, as shown in Figure 3-13.

Figure 3-14 shows the magnitude of the analog auto-zero loop gain as well as the DAC loop gain (which is inversely proportional to E). The DAC loop gain has a consistent logarithmic slope of -2, indicating that it will not be stable on its own. On the other hand, the analog auto-zero loop will be stable with $> 45^\circ$ phase margin as long as $g m_{azf} R_{az} \frac{C_{az}}{C_{int}} > 1$. The combined loop gain, which is the sum of these loops, is shown as a solid line. It levels out to a logarithmic slope of -1 before the unity-gain crossover frequency as long as $\frac{g m_{azf}}{C_{az}} > \sqrt{\frac{G_{df}}{C_{int} E}}$.

The analog auto-zero feedback loop acts as a lead compensator to stabilize the DAC feedback loop. This loop becomes less stable as it converges, because the value of E decreases, increasing the effective gain of the DAC feedback loop. It is necessary for the combined loop to remain stable until the DAC input code is within an LSB

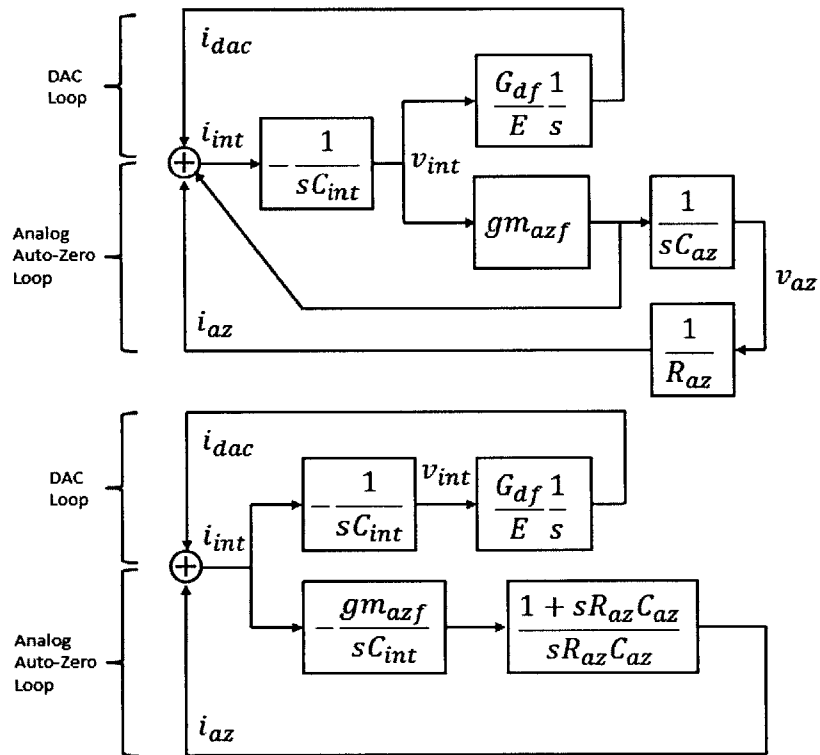


Figure 3-13: Block diagram of mixed-signal feedback loop, complete (upper) & simplified (lower)

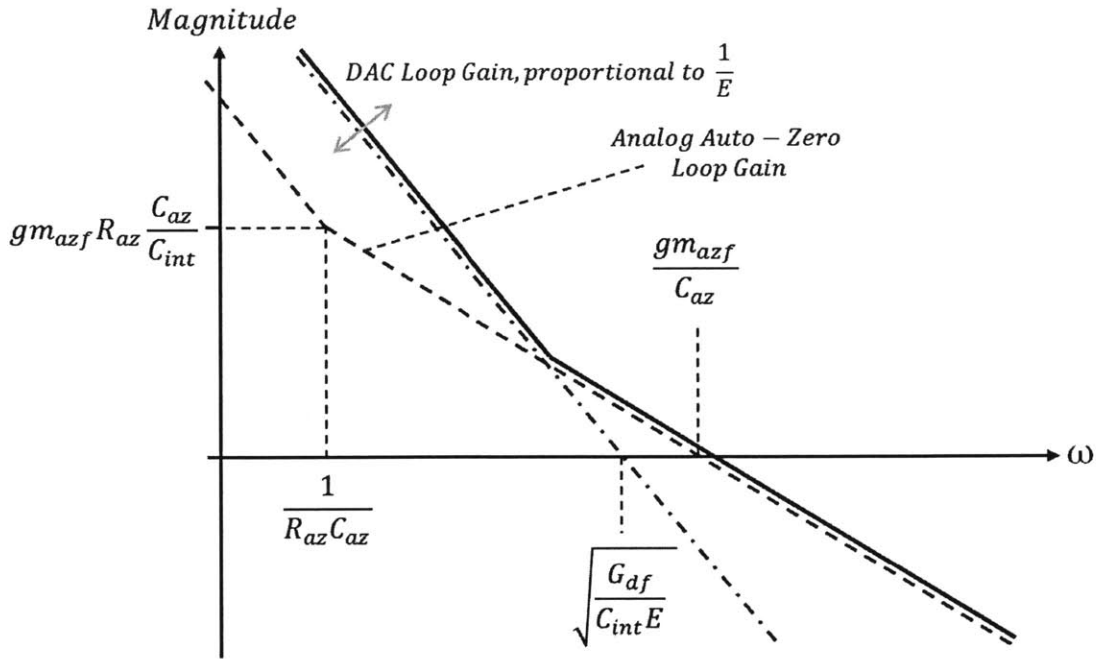


Figure 3-14: Logarithmic plot of analog auto-zero loop gain (dashed line), DAC loop gain (dash-dotted line) & combined loop gain (solid line)

of its final value, allowing the limited range of the analog auto-zero to fill in the gap.

While this method works well in the nominal case, it requires very good matching between the input offset of the comparator and gm-cell. Any mismatch will make the two feedback loops attempt to converge v_{int} to slightly different voltages. A stable point for both loops will not exist, keeping the system endlessly in oscillation. Figure 3-15 shows the DAC input code of a system with a 20mV offset between comparator and gm-cell.

Two workarounds were attempted to reduce this sensitivity - first of all, instead of being directly connected to v_{int} , the gm-cell and comparator were connected to a preamplified version of v_{int} , through a high-speed, gain-of-10 preamplifier. It was assumed that the gain of the preamplifier would reduce the effective offset of the gm-cell and comparator by a factor of 10, and they would share the input offset of the preamplifier. Unfortunately, the preamplifier's requirements of very high bandwidth, high-impedance inputs and large linear input range (equal to the full swing of v_{int}) are mutually incompatible, and this approach was abandoned.

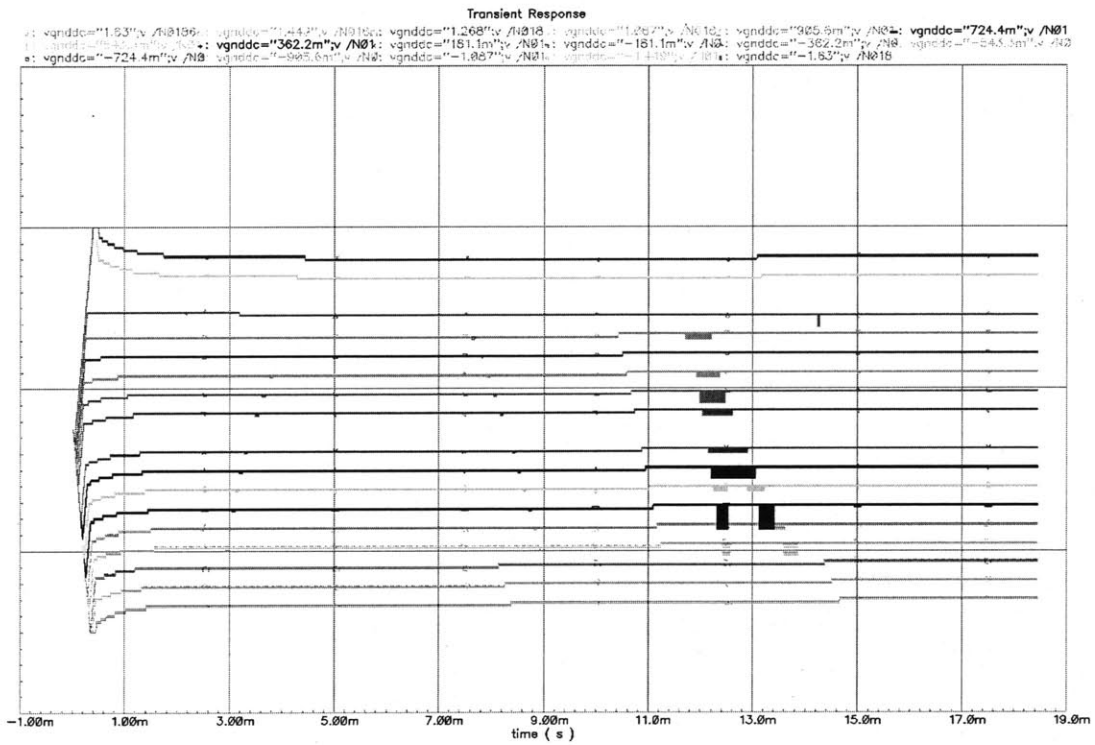


Figure 3-15: Transient simulation of mixed-signal AZ1 for various values of v_{in-} , showing DAC input code, with 20mV offset mismatch between comparator & gm-cell

The second workaround was to use two comparators, with thresholds slightly above and below the gm-cell's input offset voltage. The DAC input code was only incremented or decremented if v_{int} was above the top threshold or below the bottom threshold, creating a middle region where only the analog auto-zero is active, and the DAC feedback loop does not fight for control. This method was unsuccessful as well, because the DAC input code would drift around the final value and not converge.

Simulations suggest that the system will work with a $\leq 1mV$ offset difference between comparator and gm-cell. While large input devices are too slow for this application and trimmed input devices are too expensive, perhaps it could be done with chopped inputs for the comparator and gm-cell. This system was ultimately put aside in favor of the much simpler method below.

3.3.3 Two Measure States

While the auto-zero method described in Chapter 3.3.2 contains some interesting ideas, it is complicated and expensive. The system above relies on very well-matched components, and the gm-cell, large auto-zero capacitor, 8-bit current DAC and R_{az} resistor network considerably increase the cost of the system. This chapter discusses a much simpler idea - removing the analog auto-zero system entirely and simply having two Measure States. The first Measure State measures v_{in-} , the second Measure State measures v_{in+} , and the two digital values are simply subtracted from each other to obtain the final result. An additional $\approx \frac{v_{ref}}{2R_{ref}}$ current is added to the summing node to cancel out the average current through R_{ref} , thus biasing the range of acceptable input voltages around $v_{summingnode}$.

Figure 3-16 shows how this might be done. The switch S_{res} has been added to connect the Input Buffer to v_{ref} during AZ2 and the Residue State. The sequence of steps for pseudo-differential measurement is now as follows:

1. AZ2, to set v_{int} to the comparator threshold.
2. Measure State on v_{in-} , to measure the output down to a 12 LSB resolution.
3. Residue State on v_{in-} , to measure the mod 12 residue of the output and provide

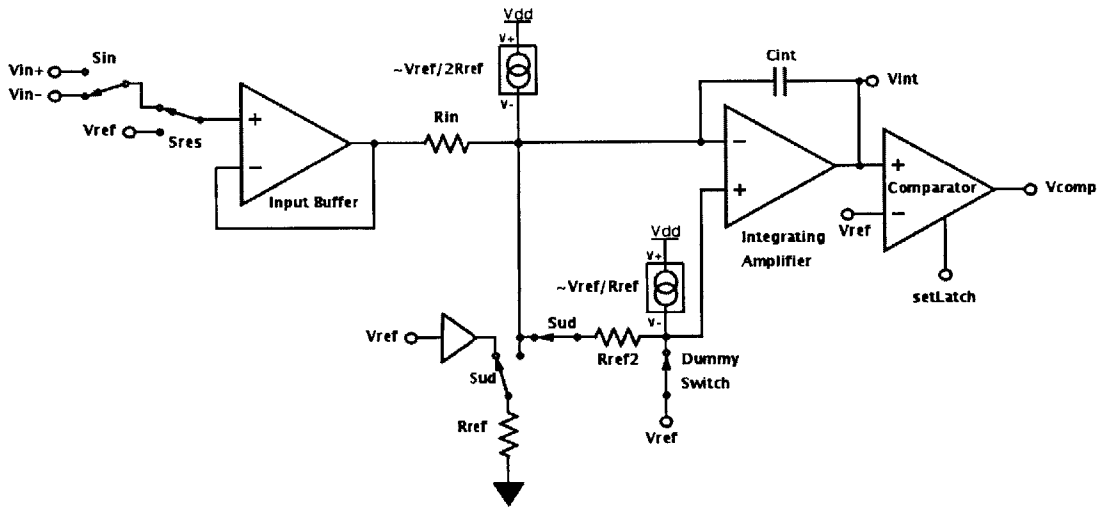


Figure 3-16: Landsburg ADC with latching comparator and without auto-zero loop

unit clock resolution.

4. AZ2, to set v_{int} to the comparator threshold.
5. Measure State on v_{in+} , to measure the output down to a 12 LSB resolution.
6. Residue State on v_{in+} , to measure the mod 12 residue of the output and provide unit clock resolution.
7. The digital output from the v_{in-} measurement is subtracted from that of the v_{in+} measurement, resulting in a differential measurement.

As the two Measure States each take 0.1s and dominate the conversion time, the entire conversion takes about 0.2s, resulting in a 5 Samples/s sampling rate. If measurements are being taken continuously, the output can be updated at the end of every Measure State (using the most recent measurements of v_{in-} and v_{in+}) to give a sampling rate of 10 Samples/s.

There are two main disadvantages which this method. The first is an increase in noise. As the final output is derived from two digital-to-analog conversions instead of one, the noise of two conversions will appear at the output. On the other hand, this is offset by the removal of the current DAC and the auto-zero buffer & resistors, all of which are significant noise sources.

The second disadvantage is a reduction of v_{in+} input range. With the auto-zero

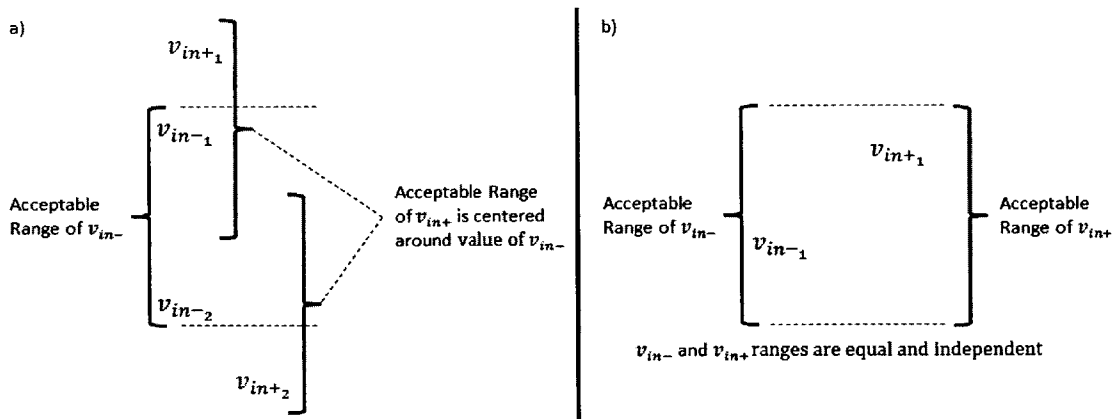


Figure 3-17: v_{in-} and v_{in+} input ranges, with (a) & without (b) auto-zero feedback loop

feedback loop, the acceptable range of voltages for v_{in+} is centered around the value of v_{in-} which was measured during AZ1. This is shown for two sets of possible v_{in-} and v_{in+} in Figure 3-17a. v_{in-1} is close to the top of the v_{in-} input range, and the v_{in+} range is centered around v_{in-1} , so v_{in+1} can be at an even higher voltage. Similarly, v_{in-2} is close to the bottom of the v_{in-} input range, and the v_{in+} range is centered around v_{in-2} , so v_{in+2} can be at an even lower voltage.

Without the auto-zero feedback loop, the v_{in+} input range is no longer centered around v_{in-} . As shown in Figure 3-17b, both v_{in-} and v_{in+} must fall within the same range of voltages, resulting in an overall decrease in the input range of the ADC.

On the upside, the removal of the auto-zero feedback loop greatly decreases the cost of the Landsburg ADC, reducing its active circuitry to two buffers, a comparator and one high-speed amplifier. Only a single moderately-large capacitor (the 50pF integrating capacitor) remains. Excluding the input buffer (which is application-specific and beyond the scope of this thesis), the estimated die area of the ADC is under $300mils^2$. With the removal of the auto-zero feedback loop, the final design resembles Figure 3-16.

3.4 Regenerative, Latched Comparator

It is necessary for the comparator output to settle well within the duration of one clock cycle. As the modified Landsburg ADC requires a 3.6MHz clock, the comparator output must settle in much less than $\frac{1}{3.6\text{MHz}} = 278\text{ns}$. This settling time is far too short for a continuous-time comparator with a current budget of under $30\mu\text{A}$. As a result, a regenerative latched comparator is used, with an output which settles within a few nanoseconds when the latch signal goes high. The rest of this section discusses the details of latch timing.

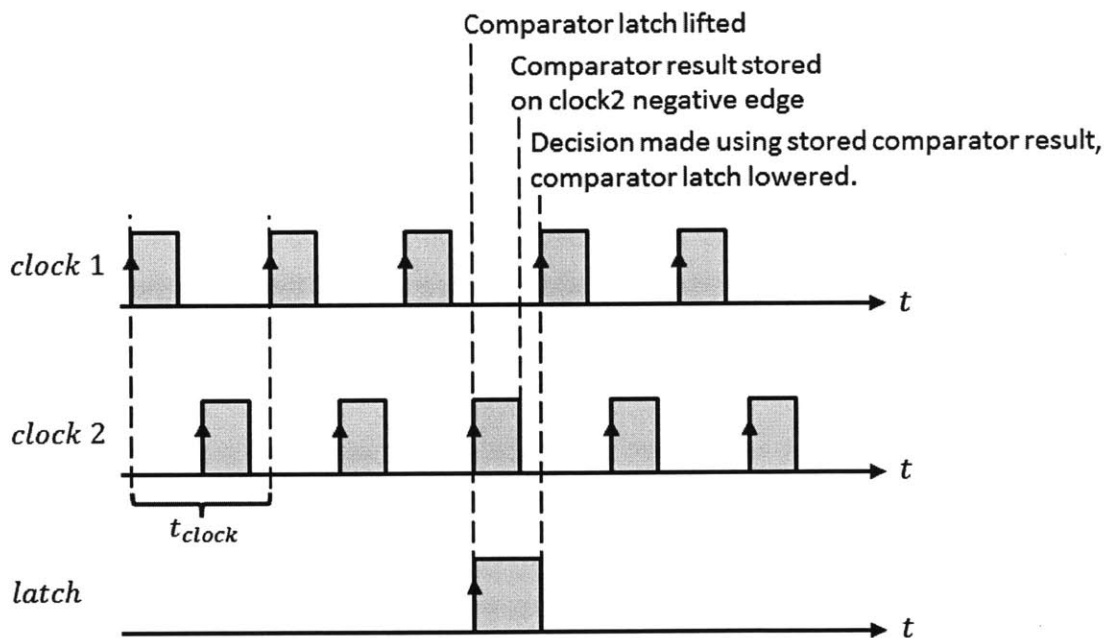


Figure 3-18: Comparator latch timing, with decision being made on the 4th clock1 rising edge

Suppose that a comparator-based decision must be made on the positive edge of a specific clock cycle. Just before this decision, the comparator latch must be lifted, and the comparator output sampled, so that a low-latency comparator output is available. Figure 3-18 illustrates a suitable timing scheme which uses a 2-phase non-overlapping clock.

If a comparator-based decision is made at the beginning of every clock cycle, as in AZ2 and the Residue State, the 'latch' pattern in Figure 3-18 will repeat every

clock cycle. During the Measure State, however, it will only repeat every m clock cycles. Recall the shape of the m -clock sequences from Figure 3-1; the first n pulses are always high, the last n pulses are always low, and the middle $(m - 2n)$ pulses are dependent on the comparator. In order to minimize latency, it is best to latch the comparator just before the 'high' and 'low' sequences deviate. In other words, during each m -clock sequence in the Measure State, the comparator is latched so that the decision can be made on the rising edge of the n th clock cycle of the sequence.

3.5 Digital Logic Tweaks

Since the introduction of the original Landsburg ADC, the cost of digital logic has fallen tremendously, justifying the use of more complicated digital controls. This chapter introduces a few changes to the digital control logic of the Landsburg ADC.

3.5.1 Residue-State Truncation

Recall the Residue State method discussed in Chapter 2.2.2. As mentioned previously, the up-integration is always performed before the down-integration to ensure that the output is always measured on the up-to-down comparator transition, which eliminates the effects of comparator hysteresis.

The generalized bounds on the residual charge, Q_{res} on the integrating capacitor are in the range of $-(m - 2n)$ to $+(m - 2n)$ clock cycles of charge. It can be assumed that v_{int} will be above the comparator threshold if you up-integrate for more than $(m - 2n)$ clock cycles. In other words, it is necessary for n_{up} to be greater than $(m - 2n)$. Similarly, $n_{down,max}$ must be greater than $(n_{up} + m - 2n)$ clock cycles to ensure that the up-to-down comparator transition occurs.

This method is suboptimal because it increases the required output swing of the integrating amplifier. Recall from Chapter 3.1.2 that the integrator output can swing as high as $v_{ref} + \frac{t_{clock}}{C_{int}} \frac{v_{ref}}{2R_{ref}} 2(m - 2n)$ during the Measure State. If, at the beginning of the Residue State, v_{int} travels upwards for a further n_{up} clock cycles, then the integrator will have to support an output swing as high as $v_{ref} + \frac{t_{clock}}{C_{int}} \frac{v_{ref}}{2R_{ref}} 2(m - 2n) +$

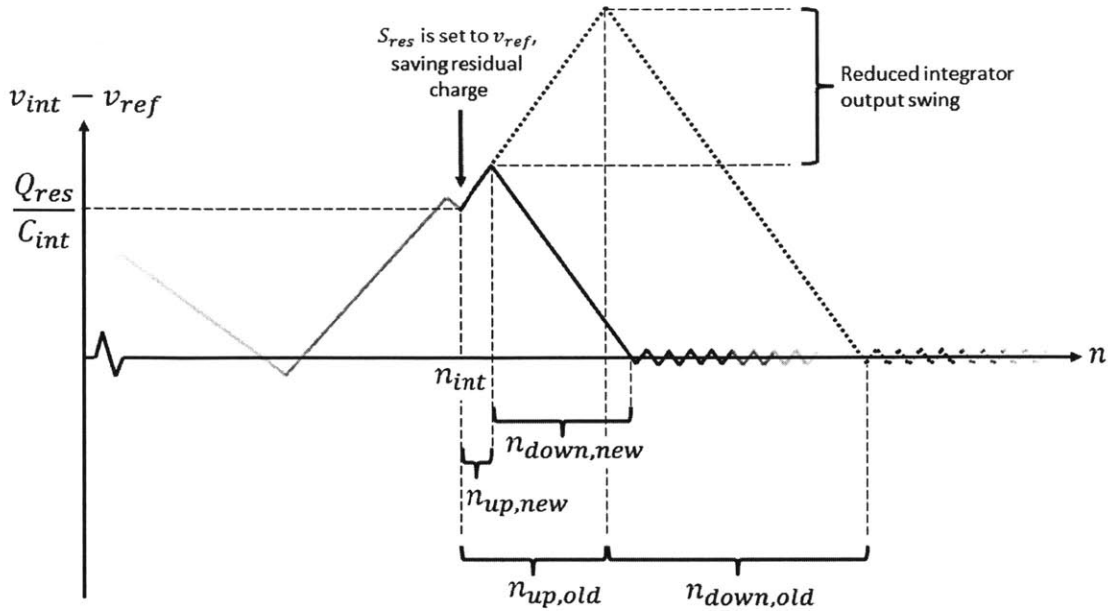


Figure 3-19: Landsburg ADC residual charge measurement, original (dotted line) & truncated (solid line)

$n_{up} \frac{t_{clock}}{C_{int}} \frac{v_{ref}}{2R_{ref}}$. Since n_{up} must be greater than $(m - 2n)$, this is a significant increase in required output swing. Figure 3-19 shows the original Landsburg design (dotted line) exhibiting this behavior.

This figure also shows the improved method, as a solid line; instead of up-integrating for a constant number of clock cycles (constant n_{up}), we truncate the up-integration and proceed to down-integration almost immediately (in this design, 4 clock cycles) after v_{int} exceeds the comparator threshold. This minimizes the required increase in integrator output swing. The overall gain is still:

$$v_{in} = v_{ref} \frac{R_{in}}{2R_{ref}} \left(\frac{14(2N_{low} - N_{integration}) + n_{down} - n_{up}}{16N_{integration}} \right)$$

However, n_{up} is no longer a constant value. It is simply as many up-integration clock cycles as is required for v_{int} to travel above the comparator threshold.

3.5.2 Overage & Underrange Detection

The modified Landsburg ADC has separate mechanisms for detect overrange and underrange conditions during the Measure State and Residue State. During the Measure State, every m -clock sequence causes a change in output code, d_{out} , of $\pm(m-2n)$. A 21-bit signed accumulator is reset at the beginning of the Measure State and used to keep a running count of these increments. If the accumulator value significantly exceeds $(2^{R-1} + m - 2n)$ for an R -bit conversion, the underrange flag is raised. Similarly, the overrange flag is raised if the accumulator value falls far beneath $-(2^{R-1} + m - 2n)$. Some safety margin is implied (the flags are raised only if the accumulator strays far outside these bounds) to make space for the input offset of the ADC.

The second overrange/underrange mechanism takes place during the Residue State. If v_{in} is within range, the residual charge, Q_{res} on the integrating capacitor should be in the range of $-(m-2n)$ to $+(m-2n)$ clock cycles of charge. It can be assumed that v_{int} will be above the comparator threshold if you up-integrate for more than $(m-2n)$ clock cycles. If v_{int} is still not above the comparator threshold after an up-integration of significantly more than $(m-2n)$ clock cycles, the overrange flag is raised. Similarly, if v_{int} is still not below the comparator threshold after much more than $(n_{up} + m - 2n)$ clock cycles, the underrange flag is raised.

Chapter 4

Circuit Design of the Modified Landsburg ADC

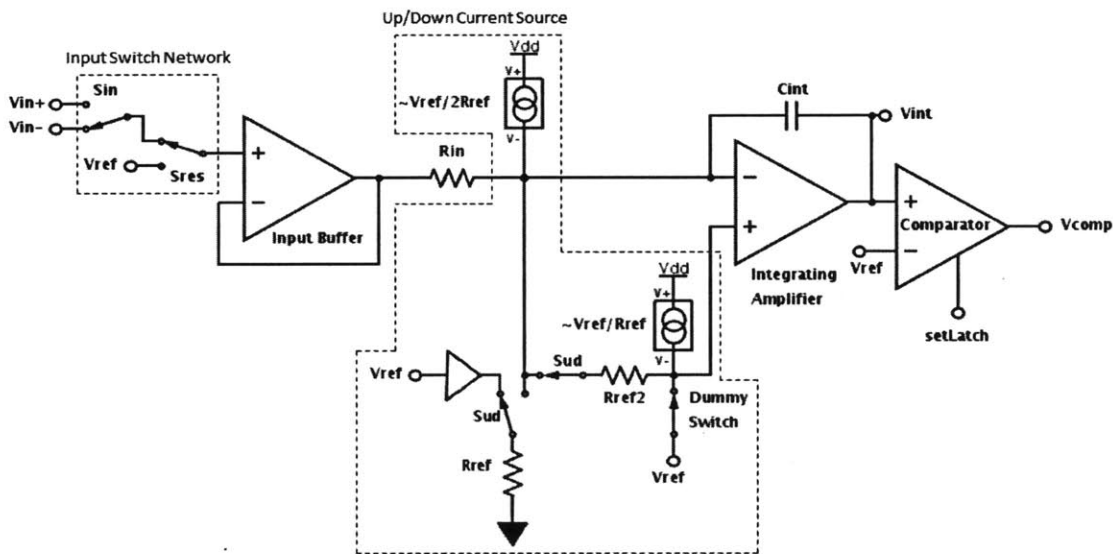


Figure 4-1: Final version of Modified Landsburg ADC with labelled blocks

This chapter describes the transistor-level circuit design of the various analog blocks in the Landsburg ADC. Except for the input buffer¹, all analog blocks are described down to transistor-level detail. Each block has been verified in simulation, across operating temperature range and $\pm 3\sigma$ device variation. Table 4.1 shows the

¹The input buffer design is beyond the scope of this thesis due to time limitations. Nevertheless, requirements for this block are discussed in Chapter 4.2.

allocation of power & area to each block.

Table 4.1: Power & Area Budget of Circuit Blocks in Landsburg ADC

Circuit Block	Power Budget (μW)	Area Budget (mils ²)
8-Bit Current DAC (removed)	200	100
Auto-Zero Buffer (removed)	125	25
Low-Leakage Switch S_{az} (removed)	-	1
Input Buffer	TBD	TBD
Input Resistor	-	4
Up/Down Current Source	325	35
Integrating Amplifier	600	25
Integrating Capacitor	-	100
Comparator	125	8
Digital Logic	250	50
TOTAL (minus Input Buffer)	1500	222

As with most designs which operate over long time-scales, we must pay attention to simulation efficiency to minimize simulation time. Each transistor-level block implementation is built in parallel with a fast-simulating block model, built from analog primitives and Verilog-AMS. As elaborated in [12], much time can be saved by simulating the full system with just one transistor-level block at a time, using simplified models for the other blocks. If certain blocks are likely to interact in a problematic way, their transistor-level implementations are tested together. Time-consuming, all-transistor-level simulations are reserved for the final verification process.

4.1 Input Switch Network

The input switch network is the implementation of switches S_{in} and S_{res} which allows us to connect the input buffer to v_{in+} , v_{in-} or v_{ref} , as shown in Figure 4-1. It is controlled by two logic signals, *input_switch* and *residue_switch*, in the manner described in Table 4.2:

While Figure 4-1 draws S_{in} and S_{res} as a pair of SPDT switches in series, it is not ideal to have two switch on-resistances in series with the input buffer. Hence the input switch network is actually implemented as a single-pole, triple-throw switch, built from three transmission gates which are controlled with break-before-make logic.

<i>residue_switch</i>	<i>input_switch</i>	Input buffer connected to
Low	Low	v_{in-}
Low	High	v_{in+}
High	Low	v_{ref}
High	High	v_{ref}

Transmission gates are used to ensure low switch on-resistance for a wide range of input voltages.

4.1.1 Transmission Gate Design

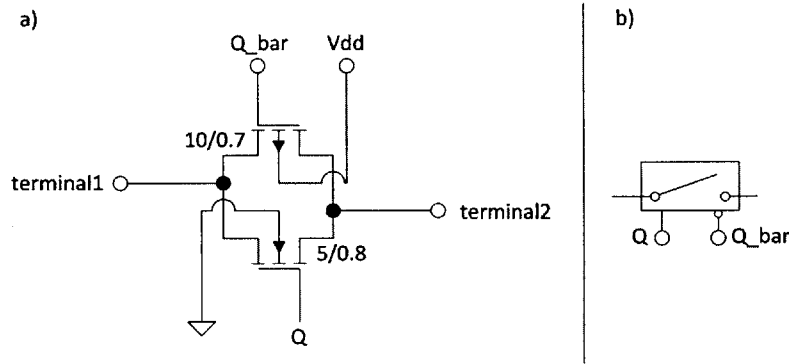


Figure 4-2: Transmission Gate design: transistor-level (a) & symbol (b)

The required on-resistance of each transmission gate can be approximated based on the input capacitance of the input buffer. Let's assume an upper bound of 1pF on this capacitance, $C_{in,inputbuffer} \leq 1pF$. Within one clock cycle, we need the input voltage to converge to 19-bit accuracy, which is equivalent to 14 time constants. With a 3.6MHz clock:

$$t_{clock} = \frac{1}{f_{clock}} \approx 280ns$$

$$\frac{t_{clock}}{14} \approx 20ns \geq R_{on,switch} C_{in,inputbuffer}$$

If $C_{in,inputbuffer} \leq 1pF$ then $R_{on,switch} \leq 20k\Omega$.

Figure 4-2 shows the design of one transmission gate, where the transistors have been sized to achieve a switch on-resistance of $< 2k\Omega$ across the input range. This

is well within the calculated $\leq 20k\Omega$ bounds. Figure 4-3 shows the transmission gate on-resistance over a $-1.25V$ to $1.75V$ switch voltage range. This is the worst-case resistance as $3V$ is the minimum supply voltage, with $v_{ref} = 1.25V$, providing the least overdrive voltage for the switches.

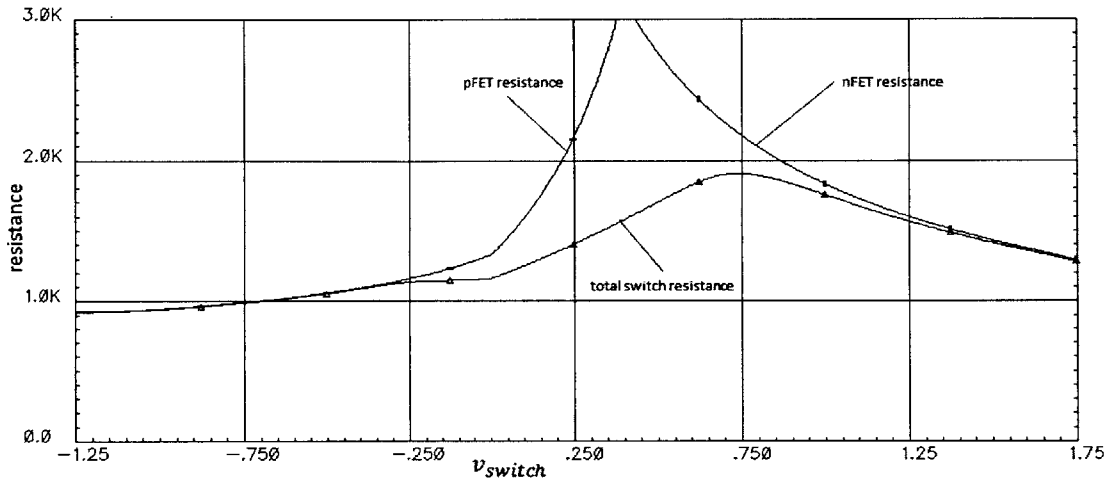


Figure 4-3: Transmission gate resistance over $-1.25V$ to $1.75V$ range

4.1.2 3-Way Break-Before-Make Logic

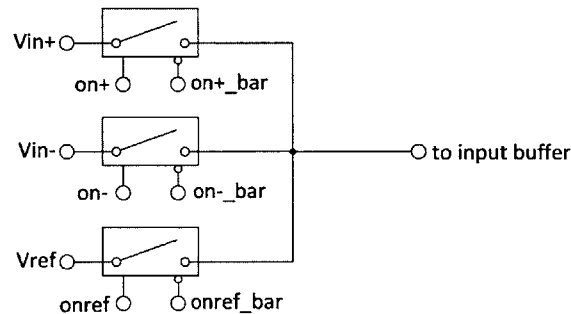


Figure 4-4: Arrangement of transmission gates in input switch network

The set of 3 transmission gates is arranged as in Figure 4-4 and controlled with logic signals $on+$, $on+_bar$, $on-$, $on-_bar$, $onref$ and $onref_bar$. These signals are controlled by break-before-make logic which ensures that only one transmission gate is on at a time. This prevents v_{in+} , v_{in-} and v_{ref} from being connected together. The

break-before-make logic takes *residue_switch* and *input_switch* as inputs and is shown in Figure 4-5.

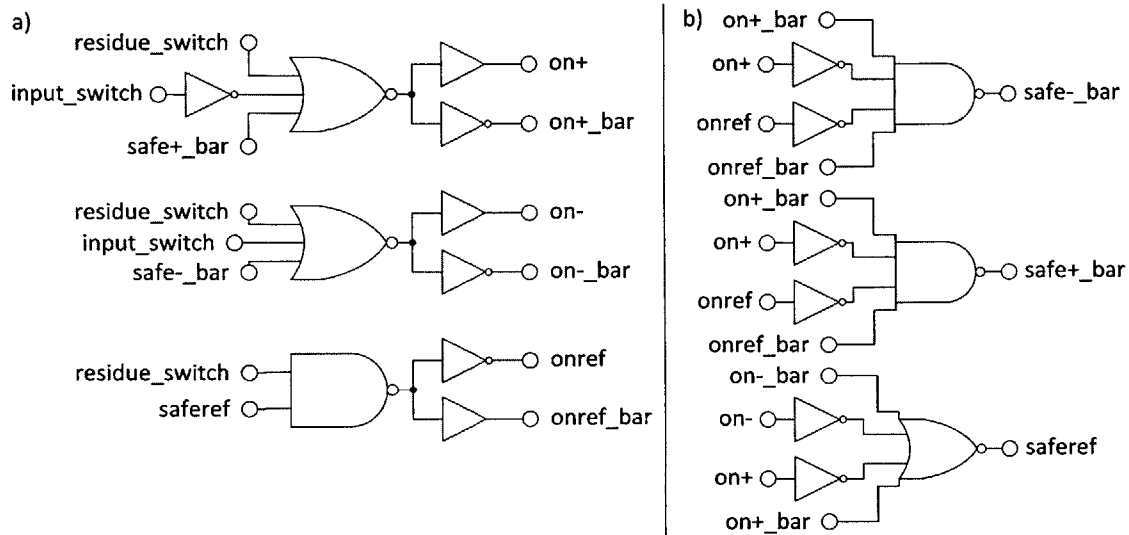


Figure 4-5: 3-Way Break-Before-Make logic: gate control (a) & break-detection (b)

Signals *safe_bar*, *safe+_bar* and *saferef* indicate when it is safe to turn on the v_{in-} , v_{in+} and v_{ref} transmission gates respectively. These signals are generated by the break-detection logic in Figure 4-5b. The gate control logic in Figure 4-5a moves the appropriate gates when it is safe to do so. Figure 4-6 shows this system in action when transitioning from v_{in+} to v_{in-} with a 3V power supply. The typical switching time from one transmission gate to another is 2-3 nanoseconds.

4.2 Input Buffer

While a transistor-level design of the input buffer is beyond the scope of this thesis, this section will describe how characteristics of the input buffer can affect the overall performance of the ADC.

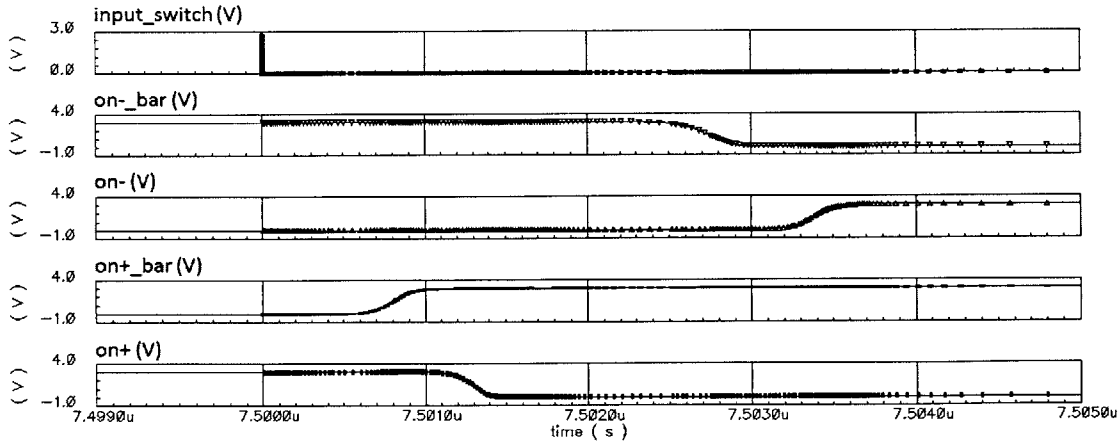


Figure 4-6: Break-before-make input transition from v_{in+} to v_{in-}

4.2.1 Input Properties

It is necessary for the input buffer to have high-impedance inputs. This is because it is preceded by the input switch network, described in Chapter 4.1, which places transmission gates in series with the front of the input buffer. These transmission gates have a non-linear, inconsistent on-resistance of up to $2k\Omega$ which forms a voltage divider with the input buffer's input. In order to prevent this inconsistent transmission gate resistance from distorting the output of the input buffer (and hence the ADC output), the input buffer must have an input impedance high enough to ignore the transmission gate on-resistance on a 19-bit level. In other words:

$$Z_{input} > 2k\Omega \cdot 2^{19} \approx 1G\Omega$$

This high impedance implies a need for MOS input devices, which carry the penalty of high $\frac{1}{f}$ noise. Since the Landsburg ADC is meant for measuring high-resolution, near-DC signals, the input buffer should have a chopped architecture to mitigate the $\frac{1}{f}$ noise of the input devices.

4.2.2 Gain & Nonlinearity

Any nonlinearity exhibited by the input buffer throughout its input range directly appears as a nonlinearity at the output of the ADC. The input buffer is a high-gain amplifier in unity gain feedback. As such, nonlinearity can be pushed below the 19-bit level as long as there is sufficient open-loop gain. Consider an amplifier with an open-loop voltage gain of A_v , placed in unity gain feedback. The input-output transfer function:

$$\frac{v_{in}}{v_{out}} = \frac{A_v}{1 + A_v} = 1 - \frac{1}{1 + A_v}$$

where the second term, $-\frac{1}{1+A_v}$, represents the deviation from ideal unity-gain behavior. Constraining this term to $\frac{1}{2}$ LSB of the ideal unity gain:

$$\left| -\frac{1}{1 + A_v} \right| < \frac{1}{2} \cdot 2^{-19}$$

$$A_v > 2 \cdot 2^{19} - 1 \approx 10^6$$

In other words, as long as the open-loop gain of the input buffer is consistently above 10^6 (120dB) throughout the input voltage range, non-linearity should be pushed below the $\frac{1}{2}$ LSB level. It is worth noting that this gain must be achieved while the input buffer is driving R_{in} , which in this design is $350k\Omega$. In order to maintain high gain while driving this load, the input buffer requires a low-impedance output stage.

4.2.3 Bandwidth & Slew Rate

Figure 4-7 shows the current through R_{in} during one instance of Measure State followed by Residue State. As the input buffer must move sharply from one near-DC voltage to another, it is assumed that slew rate effects dominate the transition time, and the transitions can be approximated as linear ramps. At the beginning of the Measure State, the input buffer's output voltage must slew from v_{ref} to v_{in+} , causing i_{in} (the current through R_{in}) to ramp up to $\frac{v_{in+}-v_{ref}}{R_{in}}$. At the end of the Measure State, i_{in} ramps back down. In the ideal case, with infinite slew rate, the total integrated charge from v_{in+} should be $\frac{v_{in+}-v_{ref}}{R_{in}}t_{meas}$, where t_{meas} is the duration of the

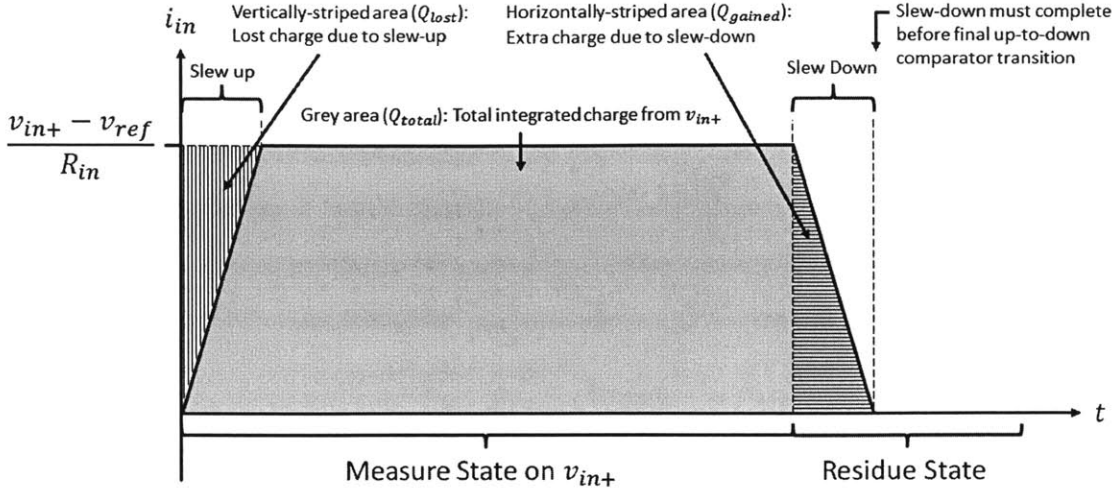


Figure 4-7: Input buffer slewing behavior during one instance of Measure State & Residue State

Measure State. Due to the finite slew rate, the actual integrated charge from v_{in+} is:

$$Q_{total} = \frac{v_{in+} - v_{ref}}{R_{in}} t_{meas} + Q_{gained} - Q_{lost}$$

If $Q_{lost} = Q_{gained}$, then $Q_{total} = \frac{v_{in+} - v_{ref}}{R_{in}} t_{meas}$ which is ideal. This is equivalent to saying that the Q_{gained} triangle will fill in the Q_{lost} triangle if they have equal area. This occurs when the upwards and downwards slew rates ($slewrates_{up} > 0$ and $slewrates_{down} < 0$) are of equal magnitude. If these slew rates are not of equal magnitude, $Q_{gained} - Q_{lost}$ is a non-zero value which introduces second-order distortion. It can be shown that the distortion from this effect, in LSBs, is:

$$INL_{slewrates} = \frac{2^R FS}{12 t_{meas}} \left(\frac{1}{slewrates_{up}} + \frac{1}{slewrates_{down}} \right)$$

where $R = 19$ is the resolution of the ADC and $FS = v_{in,max} - v_{in,min}$ is the full-scale voltage. As mentioned above, if $slewrates_{up} = -slewrates_{down}$, then $Q_{gained} = Q_{lost}$ and slew-rate distortion is zero. Hence the up & down slew rate of the input buffer must be fast enough or match well enough to push this distortion to sub-LSB levels.

Figure 4-7 shows one more criteria for the slew rate of the input buffer. It must be fast enough so that, during the Residue State, the input current can slew back to zero

before the final up-to-down comparator transition. In order to reduce the required slew rate, this time can be extended by having the up-down current source perform a net-zero-charge pattern (such as the 50% duty cycle pattern in Figure 2-8) while waiting for the input buffer to finish slewing.

4.3 Up/Down Current Source

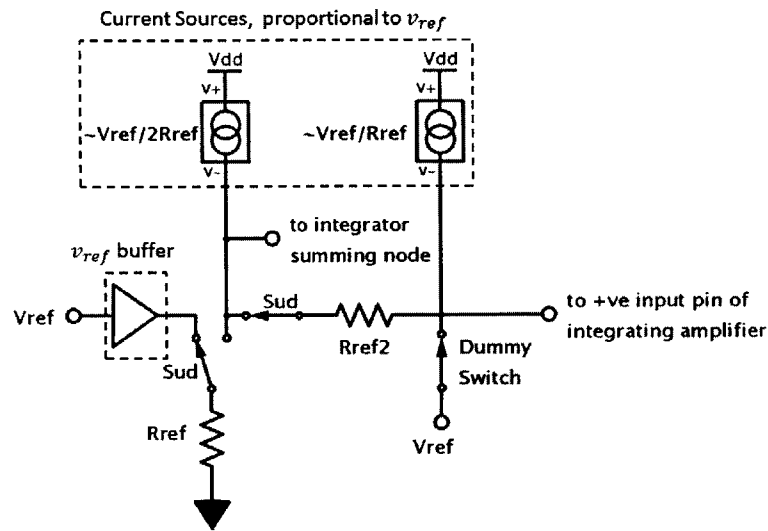


Figure 4-8: Block-level diagram of up/down current source

The up/down current source performs two functions. Depending on whether the ADC is integrating up or down (indicated by the logic signal *updown_in*), it either sinks or sources a current of $\frac{v_{ref}}{2R_{ref}}$ from the integrator summing node. It also generates the bias voltage for the integrating amplifier's positive input pin, to perform the switch resistance compensation described in Chapter 3.2.1. Figure 4-8 is a block-level diagram of the up/down current source. It consists of several switches, a v_{ref} buffer, two loosely-matched resistors (R_{ref} and R_{ref2} only require matching to $< 3\%$) and a pair of current sources which are proportional to v_{ref} .

Figure 4-9 is a transistor-level diagram of the v_{ref} buffer, current sources and bias cell. The bias cell places a voltage of $\approx v_{ref}$ across the $200k\Omega$ resistor, generating a current proportional to v_{ref} . This circuit includes an nFET as a 'turn-on device' to

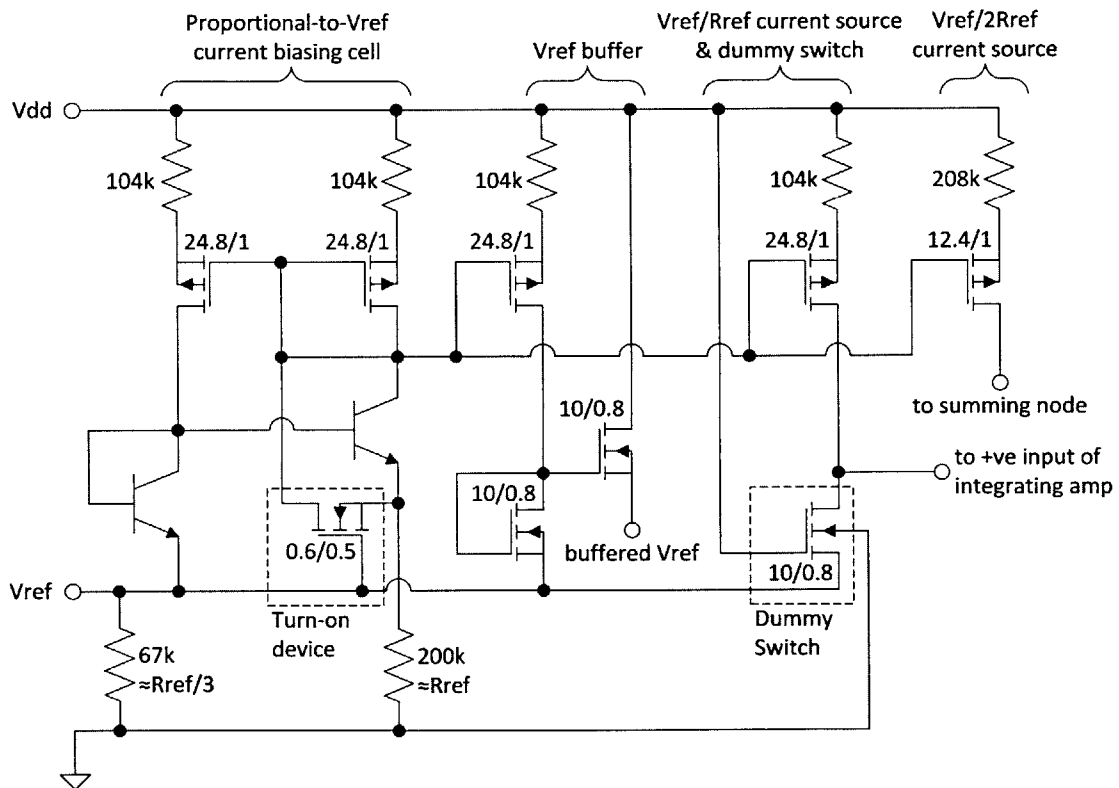


Figure 4-9: Schematic of biasing cell, v_{ref} buffer, dummy switch and $\frac{v_{ref}}{2R_{ref}}$ current source in the up/down current source

push it out of the zero-current state during turn-on. This bias current is mirrored to produce the proportional-to- v_{ref} currents in Figure 4-8. The v_{ref} buffer is built from a simple source follower. The proportional-to- v_{ref} current biasing cell, v_{ref} buffer and dummy switch each sink a current of $\frac{v_{ref}}{R_{ref}}$ into v_{ref} . The $67k\Omega \approx \frac{v_{ref}}{3R_{ref}}$ resistor drains this current from v_{ref} to minimize loading on the v_{ref} source.

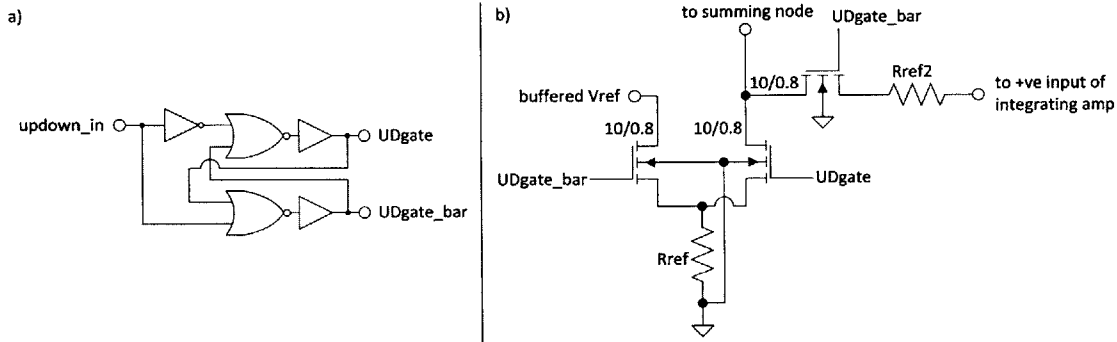


Figure 4-10: Schematic of break-before-make logic (a) and switches (b) in the up/down current source

Figure 4-10b shows the implementation of the S_{ud} switches as nFETs. Break-before-make logic is used to control these switches, as shown in Figure 4-10a. This is to ensure that the summing node is never accidentally connected to the v_{ref} buffer, which would modify the integrated charge and affect ADC linearity. This circuit is essentially a few switches connected to two resistors, where the voltage across the resistors barely changes (R_{ref} always has $\approx v_{ref}$ across it). The switching time is thus constrained to the speed of the break-before-make logic, which is $< 3ns$ across case and temp.

The current draw of the up/down current source is about $5\frac{v_{ref}}{R_{ref}}$, where $R_{ref} = 200k\Omega$. With $v_{dd} = 5V$ and $v_{ref} = 2.5V$, power consumption is about $320\mu W$. With $v_{dd} = 3V$ and $v_{ref} = 1.25V$, this decreases to $95\mu W$.

4.4 Integrating Amplifier

Figure 4-11 shows the transistor-level design of the integrating amplifier. On account of needing both high gain ($>120dB$) and bandwidth ($>25MHz$), this is the most

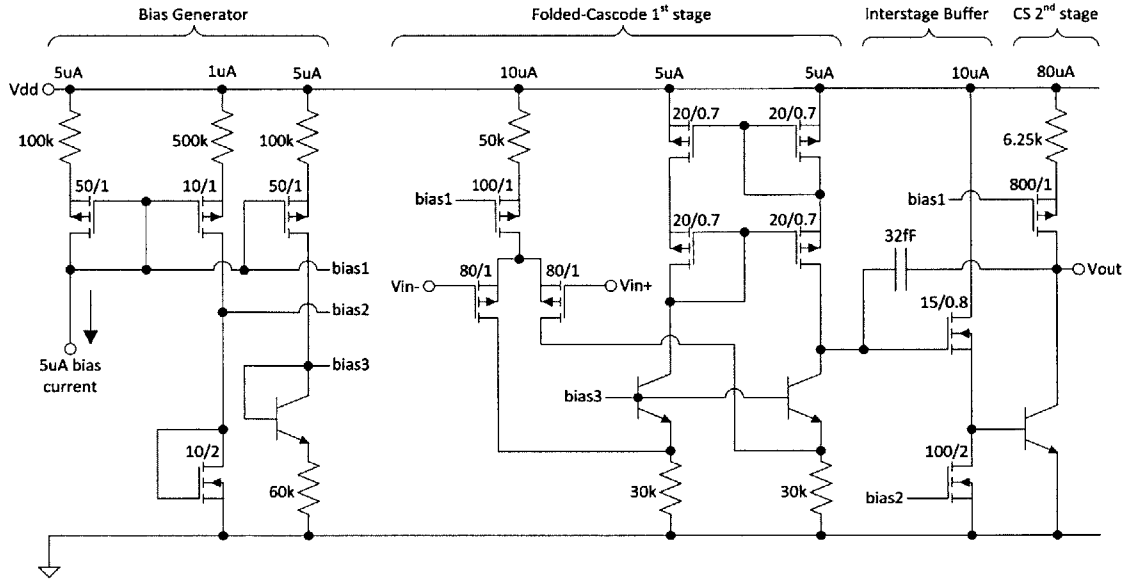


Figure 4-11: Schematic of integrating amplifier

Specification	$v_{dd} = 5V, v_{ref} = 2.5V$	$v_{dd} = 3V, v_{ref} = 1.25V$
Gain-Bandwidth Product	33MHz	32.5MHz
Phase Margin	64°	64°
Gain Margin	12.2dB	11.9dB
DC Gain	123dB	122.2dB
Power Consumption	620 μ W	370 μ W

power-hungry block in the ADC. Table 4.3 shows its nominal specifications at the upper and lower limits of its operating voltage. These specs are achieved with a two-stage Miller-compensated design. A folded cascode first-stage is used to speed up the pFET input devices by providing more v_{sd} . A buffered common-emitter second-stage is used to maximize output swing. The >120dB gain requirement necessitates that NPN transistors be used instead of nFETs, to make use of their superior transconductance and output resistance.

As covered in Chapter 3.2, the settling time of this amplifier is the main bottleneck on the speed and resolution of the ADC. Assuming completely linear behavior, the following approximation can be made about the required bandwidth of this amplifier. We need this amplifier's output to settle to <0.5LSB (<1ppm at 19-bits) within n

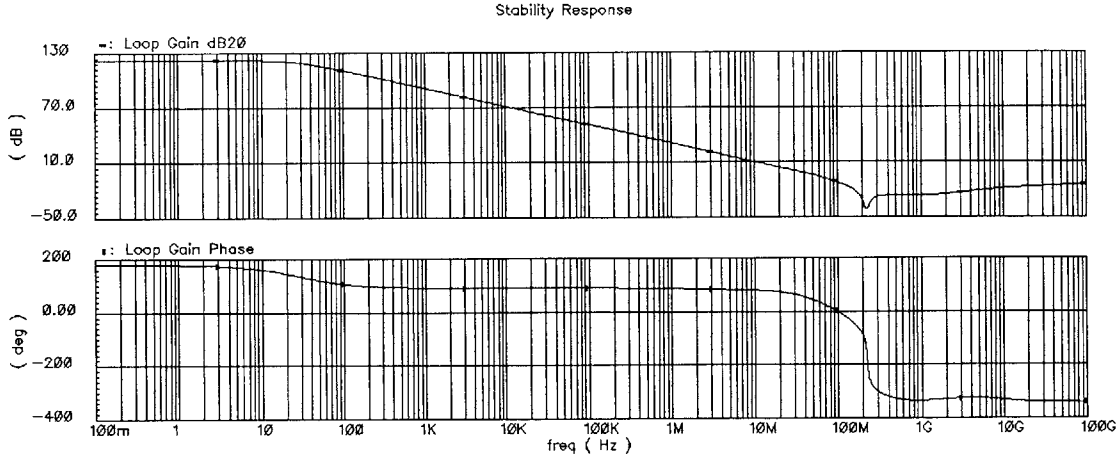


Figure 4-12: Simulated nominal frequency response of integrating amplifier, with $v_{dd} = 3V$, $v_{ref} = 1.25V$

clock cycles (as in Chapter 3.1.2). It takes about 14 time constants to settle to $<1\text{ppm}$, so the length of one time constant, τ , is:

$$\tau < \frac{nt_{clock}}{14}$$

Hence with $t_{clock} = \frac{1}{3.6\text{MHz}}$ and $n = 2$, the required bandwidth of the integrating amplifier must exceed $\frac{1}{2\pi\tau} \approx 4\text{MHz}$. This math assumes linear behavior, however, which is not realistic. In simulations with the architecture in Figure 4-11, a minimum bandwidth of 25MHz was found necessary to push INL below 1 LSB. The amplifier is designed to meet this requirement across case and temp. Figure 4-12 shows the nominal loop gain of the integrating amplifier at the lower limit of its operating voltage. Figure 4-13 shows the settling behavior of the integrator output when the integrated current switches between $\pm \frac{v_{ref}}{2R_{ref}}$ every 560ns (two clock cycles).

During testing with one transistor-level block (and the others represented with fast-simulating models), the integrating amplifier was the only block to cause discernible distortion above the quantization noise. The design shown here causes ± 1 LSB of 2nd-order distortion, due to limited bandwidth constrained by the power budget.

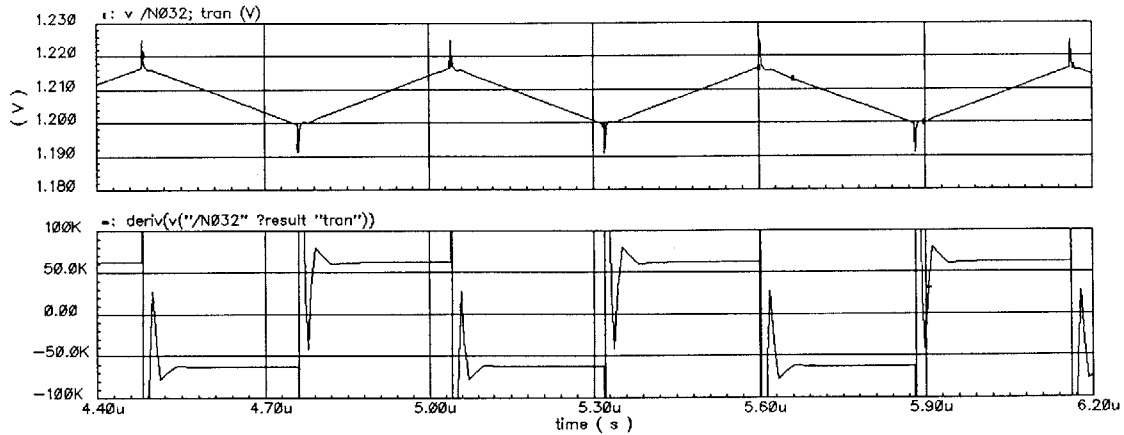


Figure 4-13: Simulated settling behavior of integrating amplifier with $v_{dd} = 3V$, $v_{ref} = 1.25V$: v_{int} (upper) and $\frac{d}{dt}v_{int}$ (lower)

4.5 Latching Comparator

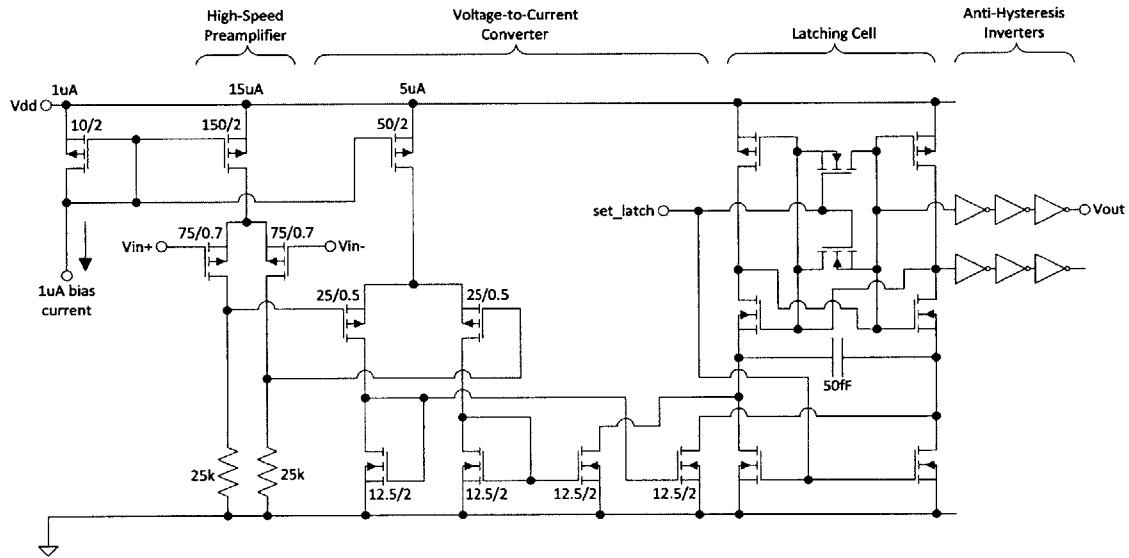


Figure 4-14: Schematic of latching comparator

Figure 4-14 shows the transistor-level design of the latching comparator. The main comparator components are the voltage-to-current converter and the latching cell. The input-referenced noise and offset voltage of these two components are attenuated by a high-speed preamplifier with a gain of 3. The 50fF capacitor across the latching cell outputs helps attenuate high-frequency noise. The output signals of the latching

cell are each buffered by three inverters before they reach the main ADC logic. This is done to present each output of the latching cell with a balanced capacitive load.

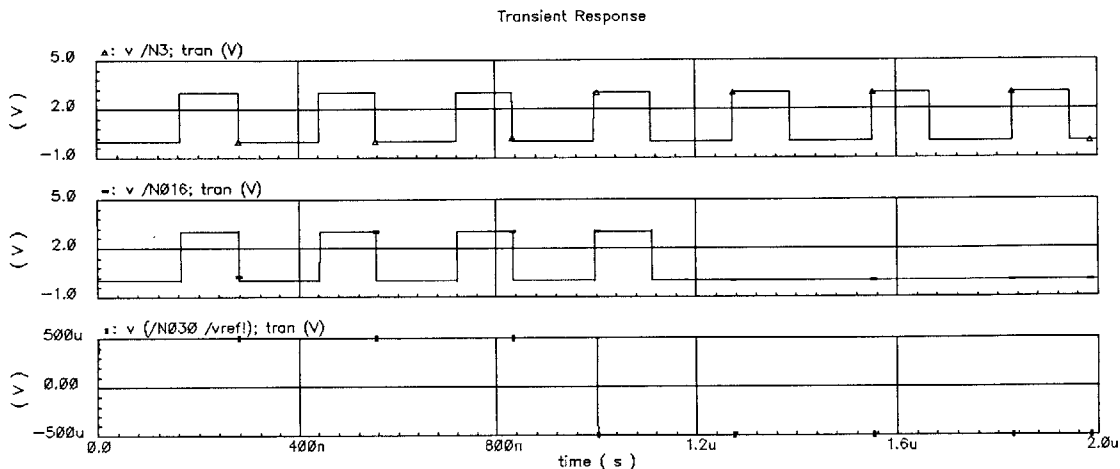


Figure 4-15: Simulation of comparator response to $\pm 0.5mV$ overdrive, with $v_{dd} = 3V$ $v_{ref} = 1.25V$: latch signal (upper), comparator output (middle) & differential input signal (lower)

Figure 4-15 shows the latching behavior of the comparator. The comparator output latches on the positive edge of the *set_latch* signal. When *set_latch* is low, the comparator output defaults to logic low. As shown in Figure 4-16, each transition takes 2-3ns, due to the regenerative action of the latched comparator. In between latch events, the current draw of the comparator is about $20\mu A$. Each latching event draws an additional 20pC of charge from the power supply. The ADC spends almost all of its time in the Measure State, during which the comparator is latched every 16 clock cycles. This results in $\frac{3.6MHz}{16} = 225000$ latch transitions per second, producing an additional current draw of $225000 \cdot 20pC \approx 5\mu A$, for a total current consumption of $25\mu A$. This results in a power dissipation of as much as $125\mu W$ when $v_{dd} = 5V$.

Figure 4-17 shows the input-referenced RMS noise of the comparator, integrated over frequency. This integrated noise levels out at $1.3mV_{rms}$. We can estimate a peak² comparator noise voltage of $6 \times 1.3mV_{rms} \approx 8mV$. As shown in Chapter 3.3.1,

² $|v_{noise}| < 6v_{noise,rms}$ is a 99.9% confidence interval on the instantaneous noise magnitude

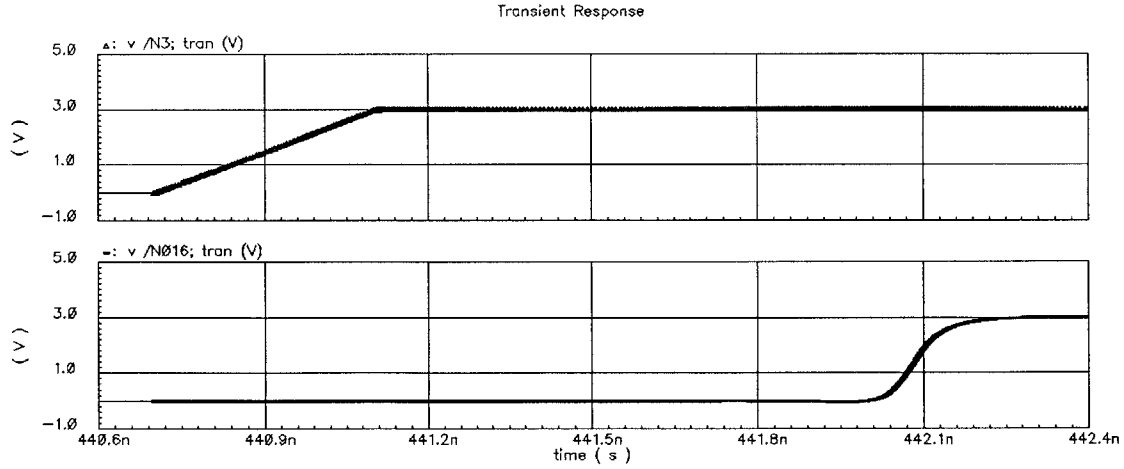


Figure 4-16: Simulation of comparator transition time, with $v_{dd} = 3V$ $v_{ref} = 1.25V$: latch signal (upper) & comparator output (lower)

the additional integrated charge from 1LSB of input voltage is:

$$Q_{int,1LSB} = \frac{1}{2^{R-1}} \frac{v_{ref} t_{meas}}{2R_{ref}} \frac{m-2n}{m}$$

Hence the difference in integrator output voltage (and hence comparator input voltage) caused by 1LSB of ADC input voltage is:

$$v_{int,1LSB} = \frac{1}{C_{int}} \frac{1}{2^{R-1}} \frac{v_{ref} t_{meas}}{2R_{ref}} \frac{m-2n}{m}$$

Using $C_{int} = 50pF$, $m = 16$, $n = 2$, $R = 19$, $R_{ref} = 200k\Omega$ and $t_{meas} = 0.1s$, we can quantify this 99.9% peak comparator noise in LSBs. With $v_{ref} = 2.5V$, $v_{int,1LSB} \approx 36mV$, and the peak comparator noise is $\frac{8mV}{36mV} \approx 0.2LSBs$ of v_{in} . Similarly, with $v_{ref} = 1.25V$, $v_{int,1LSB} \approx 18mV$, so the peak comparator noise is $\frac{8mV}{18mV} \approx 0.4LSBs$ of v_{in} .

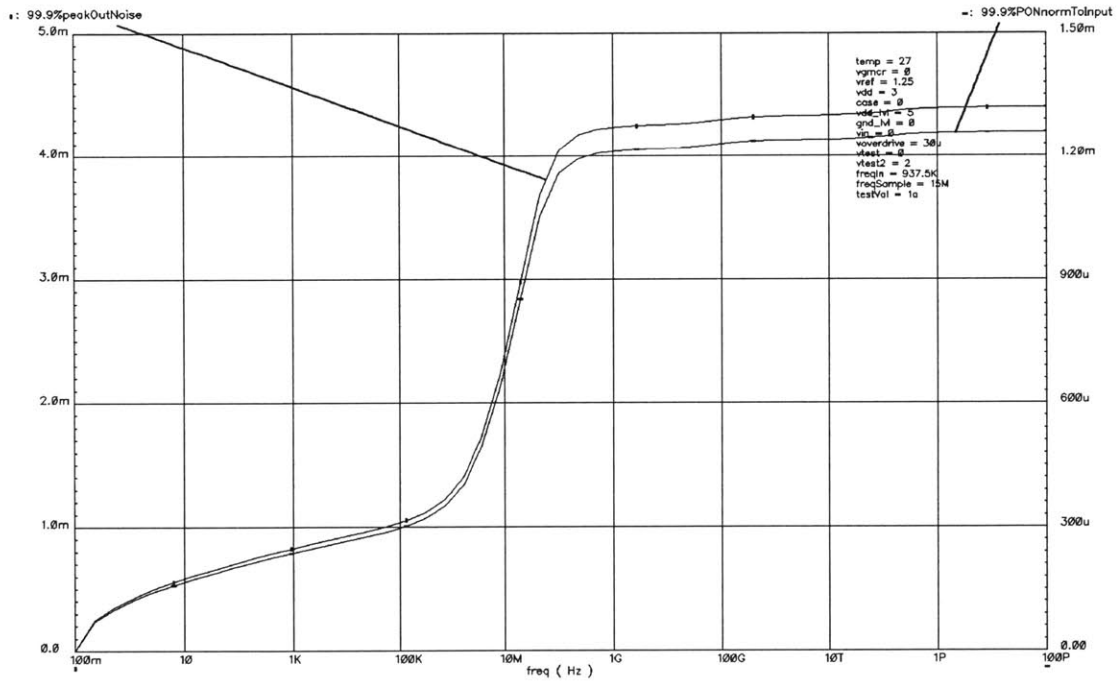


Figure 4-17: Simulation of comparator RMS noise, integrated over frequency, with $v_{dd} = 3V$ $v_{ref} = 1.25V$: across 50fF capacitor (left axis) & referenced to comparator input (right axis)

Chapter 5

Noise Analysis

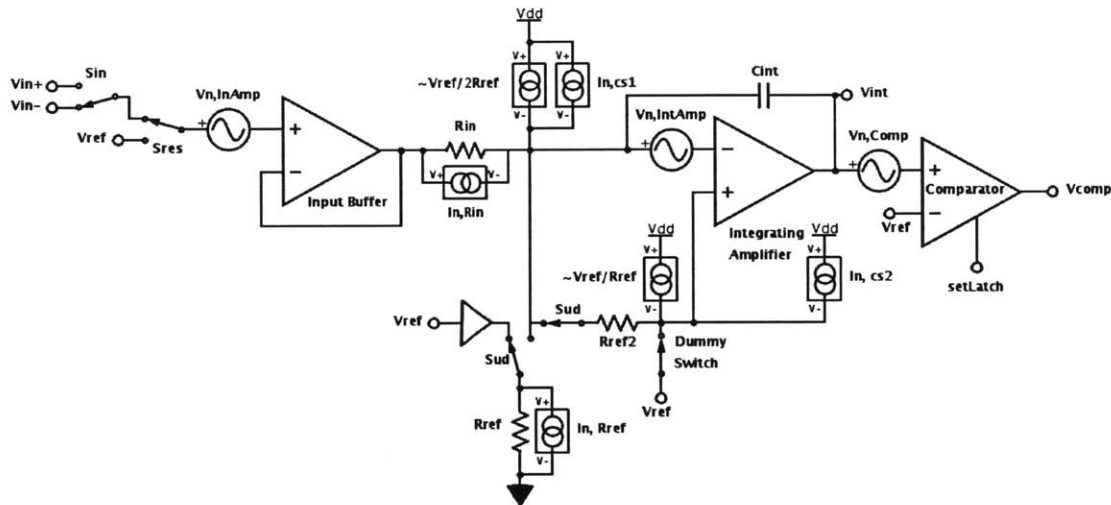


Figure 5-1: Block diagram of modified Landsburg ADC with noise sources

This chapter describes a means of calculating the total noise of the modified Landsburg ADC as a function of its internal noise sources. Figure 5-1 shows these noise sources on the block diagram of the system. They are listed as follows:

1. Input-referenced input buffer voltage noise, $v_{n,InAmp}$
2. Input-referenced integrating amplifier voltage noise, $v_{n,IntAmp}$
3. Input-referenced comparator voltage noise, $v_{n,Comp}$
4. Input resistor current noise, $i_{n,Rin}$
5. Reference resistor current noise, $i_{n,Rref}$

6. $\frac{v_{ref}}{2R_{ref}}$ current source current noise, $i_{n,cs1}$
7. $\frac{v_{ref}}{R_{ref}}$ current source current noise, $i_{n,cs2}$

The final decision of the ADC is made at the comparator, during the Residue State. In order to analyze how each noise source corrupts this decision, this chapter will reference each noise source to the input of the comparator. The comparator checks if v_{int} is greater than $(v_{ref} + v_{n,Comp})$, where $v_{int} = v_{ref} + v_{dummyswitch} + v_{n,IntAmp} + v_{C_{int}}$, $v_{C_{int}}$ is the voltage across C_{int} and $v_{dummyswitch}$ is the voltage across the dummy switch. This decision can be written as follows:

$$v_{ref} + v_{dummyswitch} + v_{n,IntAmp} + v_{C_{int}} \stackrel{?}{>} v_{ref} + v_{n,Comp}$$

$$v_{dummyswitch} + v_{n,IntAmp} + v_{C_{int}} \stackrel{?}{>} v_{n,Comp}$$

Ignoring the polarity of the noise sources:

$$v_{C_{int}} \stackrel{?}{>} v_{n,Comp} - v_{dummyswitch} + v_{n,IntAmp}$$

Assuming that the on-resistance of the dummy switch, $R_{dummyswitch} \ll R_{ref2}$,

$$v_{C_{int}} \stackrel{?}{>} v_{n,Comp} - R_{dummyswitch} \left(\frac{v_{ref}}{R_{ref}} + i_{n,cs2} \right) + v_{n,IntAmp}$$

The left and right hand side of this equation are the two ways in which the listed noise sources can distort the ADC output. On the left hand side, the integrating capacitor, $v_{C_{int}}$, samples the integrated current noise during the Measure State. On the right hand side, noise sources $v_{n,Comp}$, $v_{n,IntAmp}$ and $i_{n,cs2}$ are unaffected by the integration. The following two sections will handle these cases separately, and the third section combines them.

5.1 Integrated Noise Sources

The following table shows the current into the integrator summing node which is induced by each noise source.

Table 5.1: Integrator summing node currents induced by noise sources

Noise Source	Induced Summing Node Current
$v_{n,InAmp}$	$\frac{v_{n,InAmp}}{R_{in}}$
$v_{n,IntAmp}$	$\frac{v_{n,IntAmp}}{R_{in} R_{ref}}$
$v_{n,Comp}$	-
$i_{n,Rin}$	$i_{n,Rin}$
$i_{n,Rref}$	$i_{n,Rref}$
$i_{n,cs1}$	$i_{n,cs1}$
$i_{n,cs2}$	$\frac{R_{dummyswitch}}{R_{in} R_{ref}} i_{n,cs2}$

We can now define the total integrated noise current, $i_{n,\Sigma int}$:

$$i_{n,\Sigma int} = \frac{1}{R_{in}}v_{n,InAmp} + \frac{1}{R_{in}||R_{ref}}v_{n,IntAmp} + i_{n,Rin} + i_{n,Rref} + i_{n,cs1} + \frac{R_{dummyswitch}}{R_{in}||R_{ref}}i_{n,cs2}$$

Finding the noise power:

$$\begin{aligned} i_{n,\Sigma int}^2(f) &= \frac{1}{R_{in}^2}v_{n,InAmp}^2(f) + \left(\frac{1}{R_{in}||R_{ref}}\right)^2 v_{n,IntAmp}^2(f) + i_{n,Rin}^2(f) \\ &+ i_{n,Rref}^2(f) + i_{n,cs1}^2(f) + \left(\frac{R_{dummyswitch}}{R_{in}||R_{ref}}\right)^2 i_{n,cs2}^2(f) \end{aligned}$$

The next step is to establish the relationship between this integrated current noise, $i_{n,\Sigma int}^2$, and the sampled voltage noise across C_{int} after integrating for 0.1 seconds (the duration of the Measure State). To do this, we must understand the frequency response of an integration of 0.1 seconds. Consider the frequency-domain transfer function of integrated current (i_{int}) to integrating capacitor voltage ($v_{C_{int}}$), integrated from $-\infty$ to t :

$$v_{C_{int}} = \frac{1}{C_{int}} \int_{-\infty}^t i_{int} dt'$$

$$\frac{v_{C_{int}}(s)}{i_{int}(s)} = \frac{1}{sC_{int}}$$

If we only integrate from $(t - t_{meas})$ to t , where $t_{meas} = 0.1s$ is the duration of the Measure State:

$$v_{C_{int}} = \frac{1}{C_{int}} \int_{t-t_{meas}}^t i_{int} dt' = \frac{1}{C_{int}} \int_{-\infty}^t i_{int} dt' - \frac{1}{C_{int}} \int_{-\infty}^{t-t_{meas}} i_{int} dt'$$

$$\frac{v_{C_{int}}(s)}{i_{int}(s)} = \frac{1}{sC_{int}} - \frac{1}{sC_{int}} e^{-st_{meas}} = e^{-\frac{1}{2}st_{meas}} \frac{1}{C_{int}} \left(\frac{e^{\frac{1}{2}st_{meas}} - e^{-\frac{1}{2}st_{meas}}}{s} \right)$$

$$\frac{v_{C_{int}}(s)}{i_{int}(s)} = e^{-\frac{1}{2}st_{meas}} \frac{2}{C_{int}} \frac{\sin(\frac{1}{2}\omega t_{meas})}{s}$$

This resembles a phase-shifted sinc function, which makes sense as a time-windowed integration is equivalent to a time-convolution with a square pulse. Taking the magnitude of this function:

$$\left| \frac{v_{C_{int}}(s)}{i_{int}(s)} \right| = |e^{-\frac{1}{2}st_{meas}}| \frac{2}{C_{int}} \left| \frac{\sin(\frac{1}{2}\omega t_{meas})}{s} \right|$$

$$\left| \frac{v_{C_{int}}(f)}{i_{int}(f)} \right| = \frac{1}{\pi f C_{int}} |\sin(\pi f t_{meas})|$$

This magnitude function is plotted in Figure 5-2. As is expected of a 0.1s integration, nulls appear in the magnitude response at intervals of 10Hz. The nulls at 50Hz and 60Hz indicate the ADC's rejection of power-line frequencies. The averaging effects of the integrator also attenuate high-frequencies with a first-order roll-off. We can now calculate the sampled voltage noise across the integrating capacitor at the end of the Measure State, $v_{n,C_{int}}$:

$$v_{n,C_{int}}(f) = e^{-j\pi f t_{meas}} \frac{1}{C_{int}} \frac{\sin(\pi f t_{meas})}{j\pi f} i_{n,\Sigma int}(f)$$

Finding the noise power of $v_{n,C_{int}}$:

$$v_{n,C_{int}}^2(f) = \frac{1}{C_{int}^2} \frac{\sin(\pi f t_{meas})^2}{\pi^2 f^2} i_{n,\Sigma int}^2(f)$$

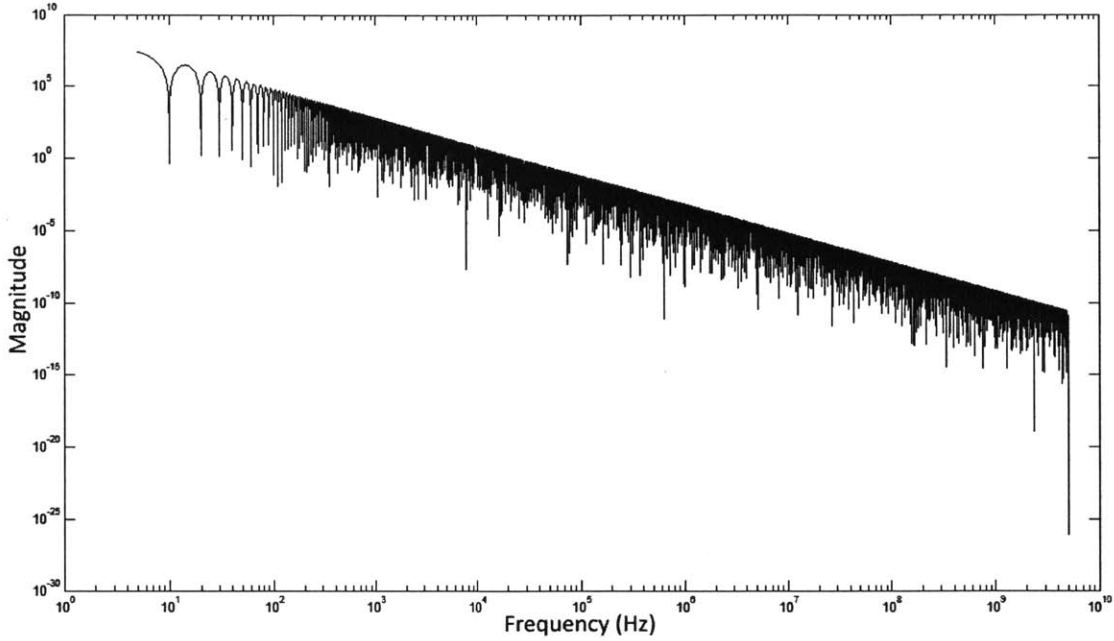


Figure 5-2: Log-log magnitude plot of $\frac{v_{C_{int}}(s)}{i_{int}(s)}$ transfer function with 0.1s integration time

$$v_{n,C_{int}}^2(f) = \frac{1}{C_{int}^2} \frac{\sin(\pi f t_{meas})^2}{\pi^2 f^2} \left[\frac{1}{R_{in}^2} v_{n,InAmp}^2(f) + \left(\frac{1}{R_{in} || R_{ref}} \right)^2 v_{n,IntAmp}^2(f) \right. \\ \left. + i_{n,Rin}^2(f) + i_{n,Rref}^2(f) + i_{n,cs1}^2(f) + \left(\frac{R_{dummyswitch}}{R_{in} || R_{ref}} \right)^2 i_{n,cs2}^2(f) \right]$$

5.2 Non-integrated Noise Sources

While Chapter 5.1 covered the sampled voltage noise across the integrating capacitor, this section will discuss the noise sources which are not attenuated by the Measure State integration. One side of the voltage across the integrating capacitor, $v_{C_{int}}$, rides on top of the summing node voltage. During comparator decisions, the other side of $v_{C_{int}}$ is compared against the comparator threshold. The non-integrated noise sources affect the comparator decision by either affecting the comparator threshold voltage or the summing node voltage. The former is the input-referenced comparator noise, $v_{n,comp}$, and the latter are $v_{n,IntAmp}$ and $i_{n,cs2}$. $v_{n,IntAmp}$ and $i_{n,cs2}$ perturb the positive input of the integrating amplifier, and the summing node voltage tracks this

perturbation due to the negative feedback of the integrating amplifier. As such, these noise sources are band-limited by the finite bandwidth of the integrating amplifier. Calculating the noise power of the total nonintegrated noise, $v_{n,nonInt}(f)$:

$$v_{n,nonInt}^2(f) = v_{n,comp}^2(f) + \frac{1}{1 + (f/GBW_{IntAmp})^2} (v_{n,IntAmp}^2(f) + R_{dummyswitch}^2 i_{n,cs2}^2(f))$$

where GBW_{IntAmp} is the gain-bandwidth product of the integrating amplifier, and we are assuming that $R_{dummyswitch} \ll R_{ref2}$. This is a conservative approximation as the integrating amplifier's limited bandwidth will band-limit $v_{n,IntAmp}$ and $i_{n,cs2}$ more aggressively than the first-order slope in the equation.

5.3 Normalized Total Noise

As established in Chapter 3.3.3, the auto-zero mechanism of the modified Landsburg ADC requires that every conversion be based on two sets of Measure State and Residue State. As such, each conversion will have the noise of two sets of Measure State and Residue State. Calculating the noise power of one conversion, referenced at the input of the comparator, $v_{n,conversion}$:

$$v_{n,conversion}^2(f) = [v_{n,C_{int}}^2(f) + v_{n,nonInt}^2(f)]_{v_{in+}} + [v_{n,C_{int}}^2(f) + v_{n,nonInt}^2(f)]_{v_{in-}}$$

$$v_{n,conversion}^2(f) = 2v_{n,C_{int}}^2(f) + 2v_{n,nonInt}^2(f)$$

Figure 5-3 shows $v_{n,conversion}^2(f)$ over frequency, based on simulated noise data from individual blocks. We can square root the area under the graph to estimate the RMS noise of the full conversion. Integrating from 2Hz to 2GHz:

$$v_{n,conversion,rms}^2 = \int_{2Hz}^{2GHz} v_{n,conversion}^2(f) df' = 0.0118V^2$$

$$v_{n,conversion,rms} = 0.109V$$

As described in Chapter 4.5, a 1LSB change in ADC input voltage produces a

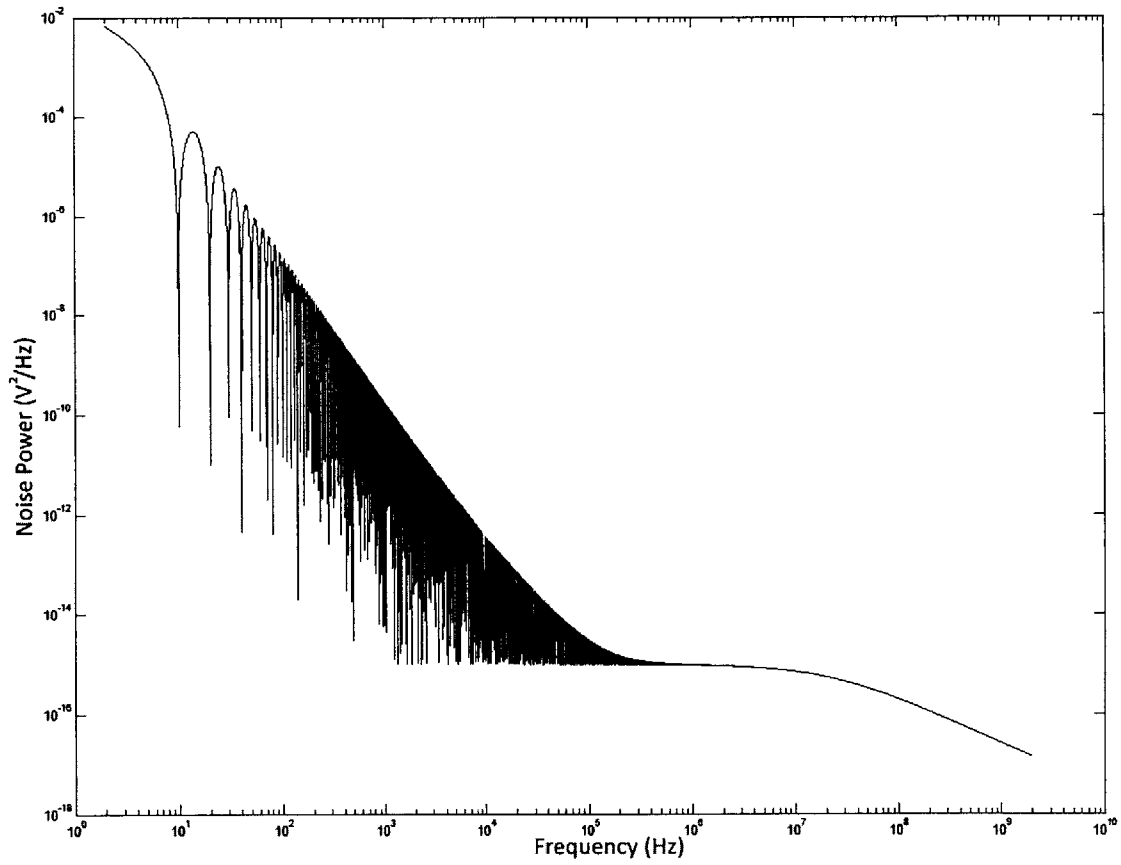


Figure 5-3: Log-log magnitude plot of total ADC noise power at comparator input, $v_{n,conversion}^2(f)$ over frequency

change of $v_{int,1LSB}$ in integrator output voltage, which can be used to normalize this noise to input LSBs:

$$v_{int,1LSB} = \frac{1}{C_{int}} \frac{1}{2^{R-1}} \frac{v_{ref} t_{meas}}{2R_{ref}} \frac{m-2n}{m}$$

Using $v_{ref} = 2.5V$, $v_{int,1LSB} \approx 36mV$. Hence $\frac{v_{n,conversion,RMS}}{v_{int,1LSB}} \approx \frac{109mV}{36mV} = 3$ input LSBs of RMS noise, which is fairly high for a precision ADC. The ENOB and SNR are as follows:

$$ENOB = \log_2 \left[\frac{2^{19} \text{LSBs}}{3 \text{LSBs} \times \sqrt{12}} \right] = 15.6 \text{bits}$$

$$SNR = 10 \log_{10} \left[\frac{(2^{19} \text{LSBs} \cdot \frac{1}{2} \cdot \frac{1}{\sqrt{2}})^2}{(3 \text{LSBs})^2} \right] = 95.8 \text{dB}$$

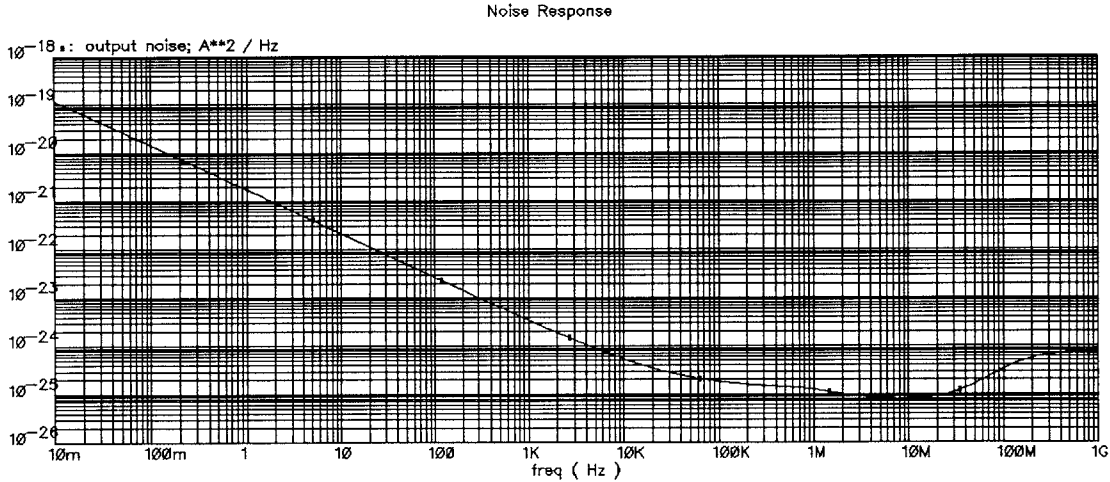


Figure 5-4: Log-log magnitude plot of noise power of the $\frac{v_{ref}}{2R_{ref}}$ current source, $i_{n,cs1}^2(f)$

Further inspection reveals the cause of this noise. It originates from the large $\frac{1}{f}$ noise current of the $\frac{v_{ref}}{2R_{ref}}$ current source, shown in Figure 5-4. Ignoring just this current source's $\frac{1}{f}$ noise results in $v_{n,conversion,rms} = 0.033V$, which is 0.92 input LSBs. ENOB (17.3 bits) and SNR (106dB) improve accordingly. This is clearly a target for future work.

Chapter 6

Conclusion & Future Work

6.1 Conclusion

In this project, an unusual charge-balancing ADC topology was revived as a fully-monolithic, high-resolution, low-cost converter. Designed and simulated on a $0.25\mu\text{m}$ CMOS process, the converter fits in under 300mils^2 of die area and produces 5 Samples/s while consuming under 2mW. The ADC has auto-zero functionality and maintains $<0.01\%$ gain error over the military temperature range. While it outputs 19-bit samples, high noise in one analog block reduces its ENOB to 15.6 bits. This should improve to >17 bits with a slight redesign.

6.2 Future Work

The modified Landsburg is still a simulated prototype. It requires an input buffer with high input impedance and low $\frac{1}{f}$ noise, suggesting a chopped MOS-input design. The excessively-noisy $\frac{v_{ref}}{2R_{ref}}$ current source (as elaborated in Chapter 5.3) begs a redesign to allow the system to meet its full potential.

As the high-gain, high-bandwidth, high-output-current requirements of the integrating amplifier are the main ceiling on the ADC's performance, it may be necessary to rearchitect the system to relax these constraints. One possibility is supplementing the integrator output's current drive with a second, complimentary up/down current

source. The integrating amplifier's gain and bandwidth might also be augmented with replica amplifier techniques[13].

Another target for future work is the inclusion of a die-level gain-calibration mechanism. As the gain is proportional to the ratio of $\frac{R_{in}}{R_{ref}}$ and R_{ref} is matched to R_{ref2} , this is best implemented as a blown-fuse adjustment of R_{in} .

Finally, the necessary steps must be taken to ready the design for fabrication. This involves layout, parasitic extraction and full system verification. We will then be able to compare theory and simulation against the ADC's real-world performance.

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